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Complementary carbon nanotube metal–oxide–semiconductor field-effect transistors with localized solid-state extension doping

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Low-dimensional semiconductors such as one-dimensional carbon nanotubes could be used to shrink the gate length of metal–oxide–semiconductor field-effect transistors (MOSFETs) below the limits of silicon-based transistors. However, the development of industry-compatible doping strategies and polarity-control methods for such systems is challenging. Here we report top-gate complementary carbon nanotube MOSFETs in which localized conformal solid-state extension doping is used to set the device polarity and achieve performance matching. The channel of the transistors remains undoped, providing complementary metal–oxide–semiconductor-compatible n- and p-MOSFET threshold voltages of +0.29 V and −0.25 V, respectively. The foundry-compatible fabrication process implements localized charge transfer in the extensions from either defect levels in silicon nitride (SiN_x) for n-type devices or an electrostatic dipole at the SiN_x/aluminium oxide (Al_2O_3) interface for p-type devices. We observe SiN_x donor defect densities approaching 5×10^{19} cm^{-3}, which could sustain carbon nanotube carrier densities of 0.4 nm^{-1} in the extensions of scaled nanotube devices. Our technique is potentially applicable to other advanced field-effect transistor channel materials, including two-dimensional semiconductors.

Semiconducting single-walled (SW) carbon nanotubes (CNTs) are an ideal channel material for scaled, high-performance transistors because of their charge carrier mobility, injection velocity and 1 nm diameter[1–7]. Recent advances in CNT transistor components have included contact resistances approaching the theoretical limit at 10 nm contact length[8], thin high-capacitance top-gate dielectrics[9] and scaled devices with record d.c. performance[10–14]. However, from a foundry perspective, record d.c. performance observed in a scaled individual device does not, in itself, indicate complementary metal–oxide–semiconductor (CMOS) relevance. A focus on modules and techniques, which can potentially leverage demonstrated d.c. performance in the complex parameter space of CMOS manufacturing, is now needed. Key aspects include device

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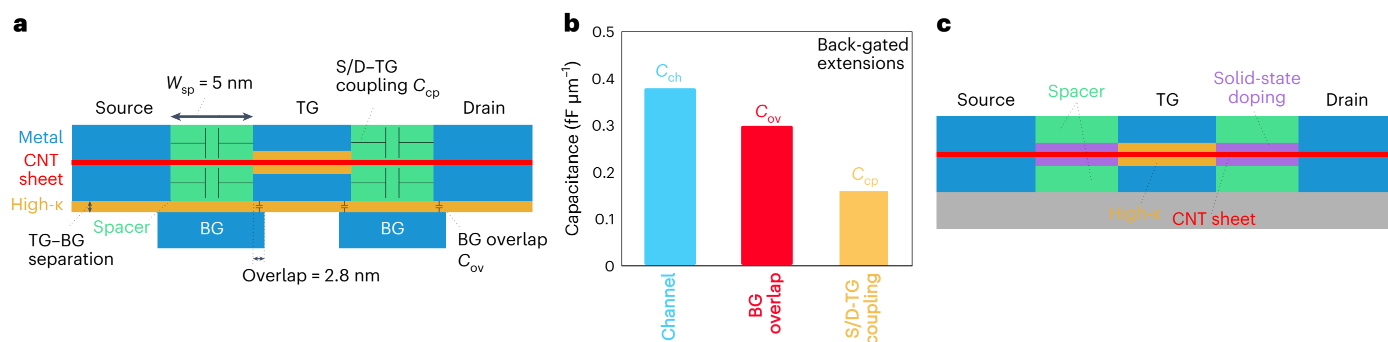

Fig. 1 | CNT device architecture comparison. a, Device architecture with local back gates (BG) to induce extension doping. **b**, Comparison of channel capacitance C_{ch} (0.37 fF μm^{-1}) with parasitic C_{ov} (0.29 fF μm^{-1}) between extension BG and top gate (TG) and parasitic coupling capacitance between gate and S/D electrodes C_{cp} (0.16 fF μm^{-1}) of architecture shown in **a**. **c**, MOSFET device architecture using localized extension all-around conformal solid-state extension doping. W_{sp} and κ are the spacer width and the relative permittivity, respectively.

architectures that minimize parasitic capacitance, device uniformity and the enablement of established CMOS metrology techniques, all of which need to be achieved while simultaneously promoting design simplicity and using standard CMOS design and process steps.

To meet the d.c. targets of the International Roadmap for Devices and Systems (IRDS)[15] for beyond 2030, including their on-current (I_{on}) and gate-length (L_g) targets, gate-all-around-like architectures will be required[2]. Global gate architectures (gate-overlapping contacts, extensions and channel) are not d.c. competitive because of a degraded above-threshold transition, leading to an I_{on} that is reduced up to three times for a given off-current I_{off} (ref. 16). Parasitic capacitance optimization and design simplicity are equally important (Fig. 1) to meet CMOS power–speed requirements. Extension doping has been identified as a key obstacle to power–speed performance because of lack of CNT-compatible, localized and foundry-friendly extension doping techniques.

However, architectures using local gates to induce extension doping (extension gates; Fig. 1a) are prohibitive because of parasitic capacitances[17] and design complexity. Using parameters from 2031 IRDS targets[15], including 3σ critical dimension control and 3σ overlay[18] (see Supplementary Fig. 1 for details), the overlap capacitance (C_{ov}) between extension back gates and the top gate is estimated to introduce a parasitic capacitance exceeding 78% of the intrinsic device channel capacitance (Fig. 1b). This analysis does not include parasitic capacitance from further routing for extension gates and increased design complexity. Additionally, because of geometrical constraints, the planar nature of extension gates and their position from the CNT sheet provides inefficient extension doping and may require non-standard CMOS voltage.

In contrast, a metal–oxide–semiconductor field-effect transistor (MOSFET) device architecture using localized extension all-around conformal solid-state extension doping (Fig. 1c) could accomplish the necessary extension doping using charge transfer from defect levels in dielectrics or a broken-gap band alignment between the dielectrics and the CNT in the extension regions only. This approach can minimize parasitic capacitance, optimize doping efficiency with an undoped channel and provide design simplicity and CMOS foundry compatibility. In particular, predictive technology computer-aided design (TCAD) modelling has shown that this MOSFET architecture could meet IRDS requirements in terms of threshold voltage V_T, I_{on}, I_{off} and subthreshold swing[19]. (A summary of key CNT device architectures previously used[16,17,20–32] is provided in Supplementary Fig. 2.)

In this article, we report top-gate complementary CNT MOSFETs on the basis of the architecture in Fig. 1c, in which device polarity is set and performance matching is achieved, using localized conformal solid-state extension doping, a module that is compatible with CMOS foundry resources. Localization of doping to the extensions only—the channel remains undoped, as in advanced silicon CMOS—is used to reduce device variability in short-channel devices. We report impedance-voltage measurements and the extraction of interface state density D_{it} as a function of gap energy. The location of interface states in energy space is essential to support identification of their structural origin and develop feasible passivation schemes. Furthermore, we use TCAD to understand the doping mechanisms and extract the density of SiN_x defects responsible for charge transfer doping. We also use TCAD to compare our experimental results with the future requirements of highly scaled devices.

CNT MOSFET fabrication, device structure and d.c. characteristics

Complementary top-gate CNT MOSFETs are fabricated on high-resistivity (2 × 10^4 Ωcm) Si wafers coated by ALD with 20 nm HfO_2. Subsequently, a high-density network of SW CNTs is deposited on the HfO_2 surface. The CNT parameters include a mean value for diameter d and length of 1.42 nm (corresponding to a bandgap of 0.55 eV) and 1 μm, respectively. The linear density is about 30 μm^{-1} (Supplementary Fig. 3). Source and drain contacts are patterned by lift-off, and palladium (Pd) contact metal is used for both n- and p-type MOSFETs[33]. The gate stack consists of low-temperature (LT) AlO_x (1.5 nm) deposited directly on the CNT network, followed by Al_2O_3 (4 nm) ALD at 250 °C and Pd gate metal (30 nm) deposition. The LT AlO_x process was previously shown to achieve conformal gate oxide coverage on CNTs while being compatible with subsequent ALD growth of high-κ dielectrics[34] and providing bilayer gate stacks with equivalent oxide thickness as low as 0.6 nm (refs. 9,34). N-type extensions are realized by electron transfer from defect levels in plasma-enhanced chemical vapor-deposited SiN_x (ref. 29) (deposition rate is about 0.13 nm s^{-1}), whereas p-type extensions rely on an electrostatic dipole at the interface of a SiN_x–Al_2O_3 bilayer. Extension doping also defines the contact polarity, avoiding the use of air exposure or process-sensitive low-working-function contact metals[35–37]. Fabricated top-gate n- and p-type MOSFETs have a gate length L_g, gate width W_g and source-drain distance L_{sd} of 1 μm, 150 μm and 3 μm, respectively. The detailed device fabrication flow is provided in Methods.

Figure 2 summarizes the structural and electrical device properties. Cross-section schematics illustrate the device structure (Fig. 2a,b), which is verified by cross-section transmission electron microscopy (TEM) (Fig. 2c,d) for both n- and p-type MOSFETs. The devices' polarity is set by the extension regions by using either a 100 nm SiN_x layer in direct contact with the CNT network (n-type MOSFET) or a 5 nm SiN_x layer situated on top of the Al_2O_3 gate dielectric stack (p-type MOSFET). Electrical n- and p-type CNT MOSFET properties (I–V) include transfer characteristics (drain current I_d versus gate-source voltage V_{gs} with source-drain voltage V_{ds} as parameter) on a logarithmic

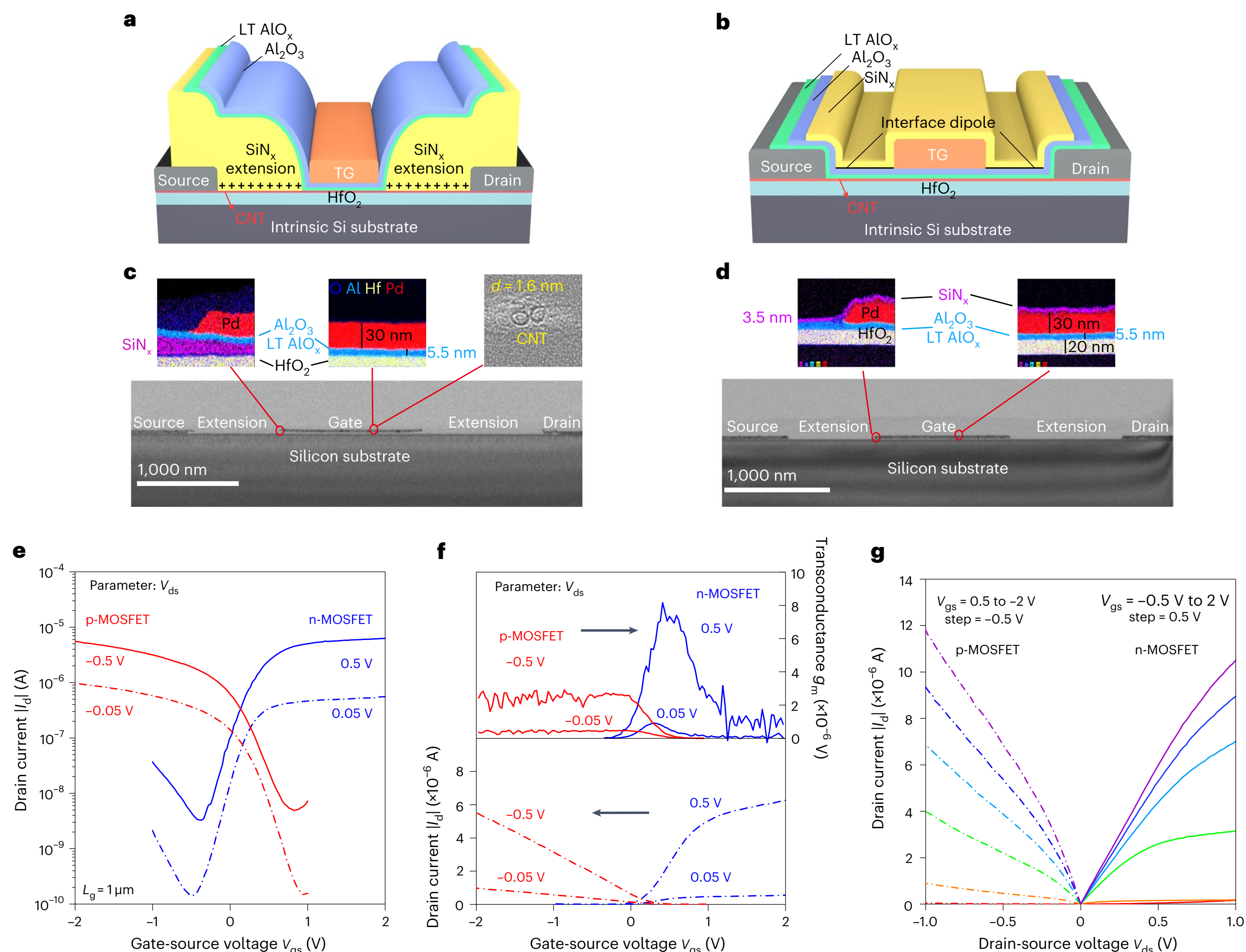

Fig. 2 | Top-gate complementary CNT MOSFETs with the devices' polarity set by localized conformal solid-state extension doping. a, Schematic of a top-gate n-type CNT MOSFET. Defects in the SiN_x at energy levels above the CNT conduction band edge E_c donate electrons to the CNT, rendering the extensions and contacts n-type, which sets the device's polarity to n-type. **b**, Schematic of a top-gate p-type CNT MOSFET. A dipole layer at the SiN_x/Al_2O_3 interface turns extensions and contacts p-type, which sets the device's polarity to p-type. **c**, TEM cross-section of a completed n-type CNT MOSFET. **d**, TEM cross-section of a completed p-type CNT MOSFET. **e**, Transfer characteristics of the complementary CNT MOSFETs at $|V_{ds}|$ = 0.05 V and 0.5 V at logarithmic scale. **f**, I_d–V_{gs} and g_m–V_{gs} characteristics of the complementary CNT MOSFETs at $|V_{ds}|$ = 0.05 V and 0.5 V at linear scale. **g**, Output characteristics I_d–V_{ds} of the complementary CNT MOSFETs with V_{gs} as parameter. The gate oxide (Al_2O_3) thickness for both n- and p-type MOSFETs is 5.5 nm.

(Fig. 2e) or linear scale with transconductance g_m versus V_{gs} (Fig. 2f) and output characteristics I_d versus V_{ds} with V_{gs} as parameter (Fig. 2g). Good performance matching between n- and p-type devices is demonstrated with V_T (0.29 V and −0.25 V), on-current I_{on} (10.5 μA, 12 μA), on-resistance R_{on} (84 kΩ, 57 kΩ) and an I_{on}/I_{off} ratio of 10^4. Here, $V_T = V_{gs}$ at maximum transconductance g_m (V_{ds} = 0.05 V), $I_{on} = |I_d|$ at $|V_{ds}|$ = 1 V and $|V_{gs}|$ = 2 V, $R_{on} = V_{ds}/I_d$ at $|V_{ds}|$ = 0.05 V and $|V_{gs}|$ = 2 V and $I_{on}/I_{off} = I_{dmax}/I_{dmin}$ at $|V_{ds}|$ = 0.05 V. Note that performance matching is accomplished with only one structural modification—the extension doping—whereas all other components including gate stack, contacts, channel and substrate are identical. The extension doping is localized, and the channel remains undoped: a key feature enabling CMOS-compatible V_T for both n- and p-type devices.

MOS impedance of one-dimensional CNT channels

Quantifying carrier density and mobility in a FET channel is key to understanding and optimizing the device's performance metrics. However, no previous experiment has directly measured the channel charge in a CNT because of the difficulty of obtaining the gate-to-channel capacitance in an environment overwhelmed by large parasitic gate-to-contacts and gate-to-substrate capacitance inherent to previously reported device architectures (Fig. 1). The carrier density has typically been estimated from electrostatic models using carrier mobility as a parameter to fit measured d.c. *I*–*V* characteristics[3,4,25]. In this study, direct measurement of the channel charge is enabled by a combination of developments that manage parasitic capacitance and minimize its effect on the measured small-signal gate capacitance C_g. These factors include a top-gate MOSFET architecture with localized solid-state extension doping, eliminating overlap of metal electrodes and associated parasitic capacitance (Fig. 2a,b); use of a high-resistivity Si substrate to minimize parasitic substrate capacitance; and on-chip zero-open and zero-short calibration structures for de-embedding measured C_g–V_g characteristics from any remaining parasitic capacitance components. With all factors above combined, C_g–V_g data are obtained with high confidence over a frequency range *f* of 100 kHz to 1 MHz.

Figure 3a shows scanning electron microscope images of layouts for CNT capacitor and on-chip zero-open and zero-short calibration

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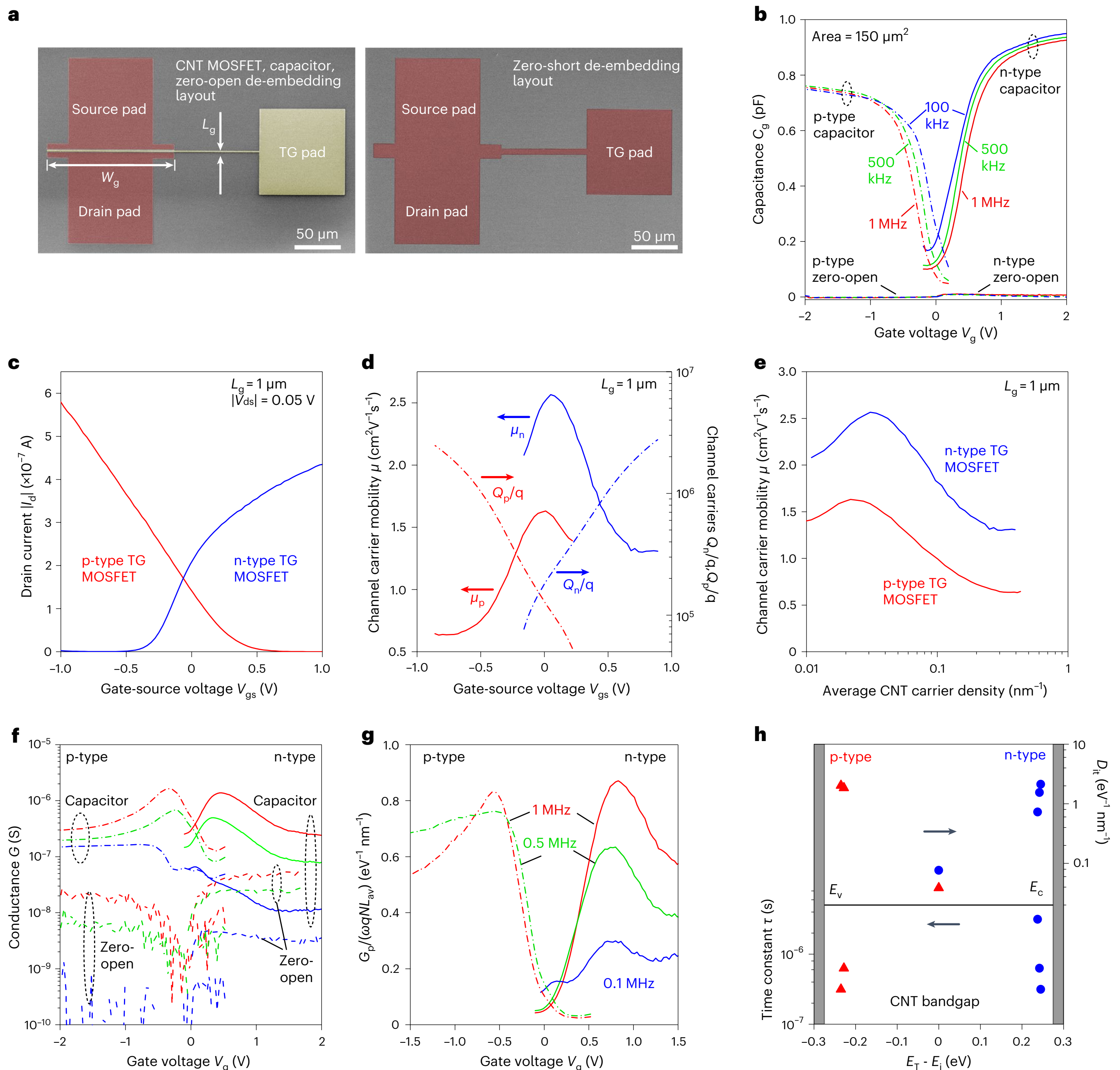

Fig. 3 | Device layout, capacitance-voltage characteristics, channel-carrier mobility and density. a, False-colour scanning electron microscope pictures of device layouts. The layout of the TG CNT MOSFET and the CNT capacitor are identical; the zero-open de-embedding structure shares the same visible layout elements (left). For MOSFET I_d–V_{gs} measurements, $|V_{ds}|$ = 0.05 V. Both source and drain terminals are grounded during C_g–V_g measurements. L_g and W_g are 1 μm and 150 μm, respectively. Zero-short de-embedding structure (right). **b**, Multifrequency C_g–V_g characteristics of CNT capacitors and of zero-open de-embedding structures after zero-open and zero-short calibration. **c**, CNT MOSFET I_d versus V_{gs} transfer curves at $|V_{ds}|$ = 0.05 V. **d**, Channel-carrier mobility μ and channel-carrier density Q as a function of V_{gs}. **e**, Channel-carrier mobility μ as function of average carrier density n or p of an individual CNT. Maximum network channel mobility μ_n of 2.6 cm² V⁻¹s⁻¹ and μ_p of 1.6 cm² V⁻¹s⁻¹ is observed at an average carrier density of an individual CNT n = 0.031 nm⁻¹ and p = 0.022 nm⁻¹ for n-type and p-type MOSFETs, respectively. **f**, Multifrequency G–V_g characteristics of CNT capacitors and zero-open de-embedding structures after zero-open and zero-short calibration. The measurement frequencies are 1, 0.5 and 0.1 MHz, indicated with red, green and blue colour, respectively. **g**, Parallel conductance of interface states of CNT capacitors as a function of V_g. **h**, Interface state density D_{it} and corresponding characteristic time constant τ as a function of $E_T - E_i$ in the CNT bandgap.

structures. Note that the capacitor layout differs from the zero-open calibration structure only by the presence of CNTs in the active area of the capacitor; visible layout elements are identical. The capacitor layout also matches that of the MOSFET; the difference here is in the measurement condition. After completion of zero-open and zero-short calibration using the on-chip calibration structures, multifrequency ($0.1 \le f \le 1$ MHz) C_g–V_g characteristics of CNT capacitors and zero-open calibration structures are measured (Fig. 3b). N- and p-type zero-open structures measure a capacitance not exceeding 10 fF (Fig. 3b), keeping parasitic capacitance at 1–10% of CNT gate capacitance over the studied

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gate-voltage and frequency range. To obtain carrier mobility, further data required are MOSFET I_d–V_{gs} curves at low V_{ds} (Fig. 3c) and parasitic device resistance R_p, which is derived from resistor I–V measurements (Supplementary Fig. 4).

The total measured carrier density under the gate $Q = \int C_g dV_g$ where 1 MHz C_g–V_g curves are used to minimize the effect of trapped charge on Q. The channel-carrier mobility is obtained using $\mu = I_d L_g^2 / Q V_{ds,int}$ (ref. 38) where the intrinsic voltage $V_{ds,int} = V_{ds} - I_d R_p$. Figure 3d shows the channel-carrier mobility μ_n, μ_p and the channel charge Q_n, Q_p of the CNT network as a function of V_{gs} for n- and p-type CNT MOSFETs, respectively. Channel-carrier mobility μ_n, μ_p versus average carrier density n and p of individual CNTs for n- and p-type MOSFETs is shown in Fig. 3e. The carrier densities observed in an individual CNT are obtained using $n = Q_n/(N_n L_{av} q)$ and $p = Q_p/(N_p L_{av} q)$, where N_n and N_p are the number of CNTs, L_{av} is the average CNT length under the gate and q is the unit charge. N_n and N_p are estimated using the ratio between total measured accumulation capacitance (9.2×10^{-13} and 7.5×10^{-13} F for the n- and p-type MOSFET, respectively) and the average CNT accumulation capacitance per unit length $C'_{mod} = 1.31 \times 10^{-10}$ F m^{-1} for the gate stack in Fig. 2, as calculated from electrostatic models[39] and the CNT density of states[40] (Methods). The values obtained are $N_n = 4{,}966$ and $N_p = 4{,}048$ for the n- and p-type MOSFET, respectively. The corresponding linear CNT densities are $N_n/W_g = 33$ and $N_p/W_g = 27$ µm^{-1}, which are in good agreement with the CNT density obtained from atomic force microscopy measurement (Supplementary Fig. 3). Note that for a CNT network, the carrier mobility including its peak position is determined by the conductivity of junctions connecting the CNTs and is not representative of the intrinsic CNT carrier transport. However, the demonstrated technique can be readily applied to high-purity, high-density, well-aligned CNTs when such substrates become available to experimentally obtain intrinsic CNT carrier mobility versus carrier density.

The ability to measure gate-to-channel impedance including C–V and conductance-voltage (G–V) characteristics further enables the extraction of density and characteristic time constants of electronic states located at the interface between a CNT and the gate oxide. Figure 3f shows multifrequency G–V_g characteristics of CNT capacitors and zero-open de-embedding structures. Note that the parasitic conductance signal obtained from zero-open structures is typically two to three orders of magnitude below the signal observed on the CNT capacitors. Conductance peaks, the hallmark of interface states, are only found on CNT capacitors, which provides further evidence that the conductance signal originates from the interface between the CNTs and the gate oxide. Interface state parallel conductance G_p is obtained from measured capacitance C_g and conductance G[41]. Figure 3g shows the normalized interface state parallel conductance $G_p/(\omega q N L_{av})$ of an individual CNT, where ω and N are the angular frequency and number of CNTs under the gate, respectively. Density D_{it} and characteristic time constant τ of interface states are obtained from the peak value of each curve[41] and are summarized in Fig. 3h as a function of the energy level E_T of an interface state relative to the intrinsic energy level E_i of the CNT. Interface states densities of 1–3 eV^{-1} nm^{-1} are observed in the vicinity of the band edges of an individual CNT with time constants around 1 µs.

The frequency dispersion observed in the measured C_g–V_g curves (Fig. 3b) is further used to obtain a first D_{it} estimate in the vicinity of E_i using the measured frequency dispersion at the capacitance minimum by applying the combined high-low frequency capacitance method[41]. For a single CNT, D_{it} values of 0.076 and 0.039 eV^{-1} nm^{-1} are obtained for n- and p-type capacitors, respectively. Note that the derived density is a lower limit because further frequency dispersion is to be expected below 100 kHz.

Localized and tunable doping polarity for n- and p-type MOSFET extensions

Localized and tunable doping providing both n- and p-type polarity is a key ingredient of the MOSFET architecture presented in Fig. 2. Experimental evaluation of doping efficiency is on the basis of global back-gate FETs, and doping quantification leverages electrostatic models. Cross-section schematics of CNT FETs used to develop n- and p-type solid-state doping are shown in Fig. 4a,b, respectively. All devices consist of a p$^+$ silicon back gate separated from the CNT network channel by a 15 nm HfO_2 film. The separation of the Pd contacts defines the gate length (1 µm); the device width is 50 µm. The FET polarity is determined by dielectric films subsequently deposited on top of the CNT network and simultaneously on the entire device, providing global doping.

For n-type doping, single SiN_x films are deposited under different conditions including deposition time, optimized NH_3 and SiH_4 flow rates and NH_3/SiH_4 flow ratio $R = 3$ (set A), whereas p-type doping is observed by depositing a SiN_x–LT AlO_x bilayer using $R = 3$ and 100 (set B). In Fig. 4c, selected I_d versus V_{gs} curves ($V_{ds} = 50$ mV) are shown for both sets A and B. Typically, flatband voltage shift ΔV_T has been used to quantify doping. In an ideal device, all points along the I_d–V_{gs} curve are shifted by the same amount of V_{gs}, and any point can be chosen to quantify doping. We found ΔV_T to be less suitable for doping quantification because of strong charge trapping at V_T (the Fermi level E_F is located close to the CNT band edge, where a large trap density resides) and a notable effect from Schottky barriers at contacts for high current levels. Both parameters above introduce further doping-dependent shifts and stretch out of the I_d–V_{gs}, making quantitative extraction of doping density difficult. Here, we introduce the metric V_{min}, with $V_{min} = V_{gs}$ at minimum I_d. V_{min} is a distinct bias point with underlying physical meaning where the ambipolar device switches from one polarity to the other and the channel Fermi level resides at the intrinsic level E_i. We found V_{min} to be not only an important quantity to identify the type of doping, the relative doping strength and quantitative doping parameters (discussed further below), but also a highly relevant metric for de-embedding doping effects from other mechanisms such as trapped charge (which is minimal at E_i because of either emission or neutralization (by means of recombination) of charge previously captured at the CNT band edge) and the effect of Schottky barriers at contacts, which is minimized at low current levels[42,43]. The position of V_{min} is indicated on the I_d–V_{gs} curves in Fig. 4c. When a single SiN_x film is deposited (set A, n-type doping), V_{min} shifts to more negative values with increasing SiN_x deposition time; this is accompanied by formation of a stronger n-type branch, whereas the p-type branch gradually disappears. However, when a SiN_x layer is deposited on LT AlO_x, forming a bilayer (set B), a positive V_{min} shift is obtained, resulting in p-type doping with reinforced p-type and suppressed n-type branch.

Next, the metric ΔV_{min} is introduced with $\Delta V_{min} = V_{min} - V_{ref}$, where $V_{ref} = V_{min}$ of the undoped reference case. The voltage of the undoped reference case V_{ref} is set by the intrinsic energy level E_i of the CNT with $V_{ref} = E_F - E_i = (5.17\ \text{eV} - 4.5\ \text{eV})/q = 0.67$ V, where E_F is the Fermi energy of the back-gate p$^+$ Si substrate. On the basis of the definition of V_{ref}, n-type and p-type doping is observed for $\Delta V_{min} < 0$ and $\Delta V_{min} > 0$, respectively. In Fig. 4d, a summary of experimentally obtained ΔV_{min} data is shown as a function of SiN_x deposition time for both single SiN_x films and SiN_x–LT AlO_x bilayers. For all samples, ΔV_{min} continues to decrease with increasing SiN_x deposition time over the entire range experimentally investigated. Because only SiN_x defect levels in the vicinity of the CNT contribute to doping of the CNT (further discussed below), we consider that continuing changes of composition and atomic-bonding structure in the initially deposited SiN_x layer are likely facilitated by diffusion of species towards the interface, leading to increased SiN_x defect density in the immediate vicinity of the CNT and the SiN_x–HfO_2 interface as SiN_x deposition continues. For deposition of a SiN_x–LT AlO_x bilayer, the ΔV_{min} versus SiN deposition time dependence is shifted along the ΔV_{min} axis by +1.5 V, indicating the presence of an electrostatic dipole at the SiN_x–LT AlO_x interface. Note that similar dipole layers were reported earlier at SiO_2–Al_2O_3 interfaces[44].

To explain the experimentally observed dipole, models including an oxygen-density-difference model[44] and oriented Al–O–Si bonds[45]

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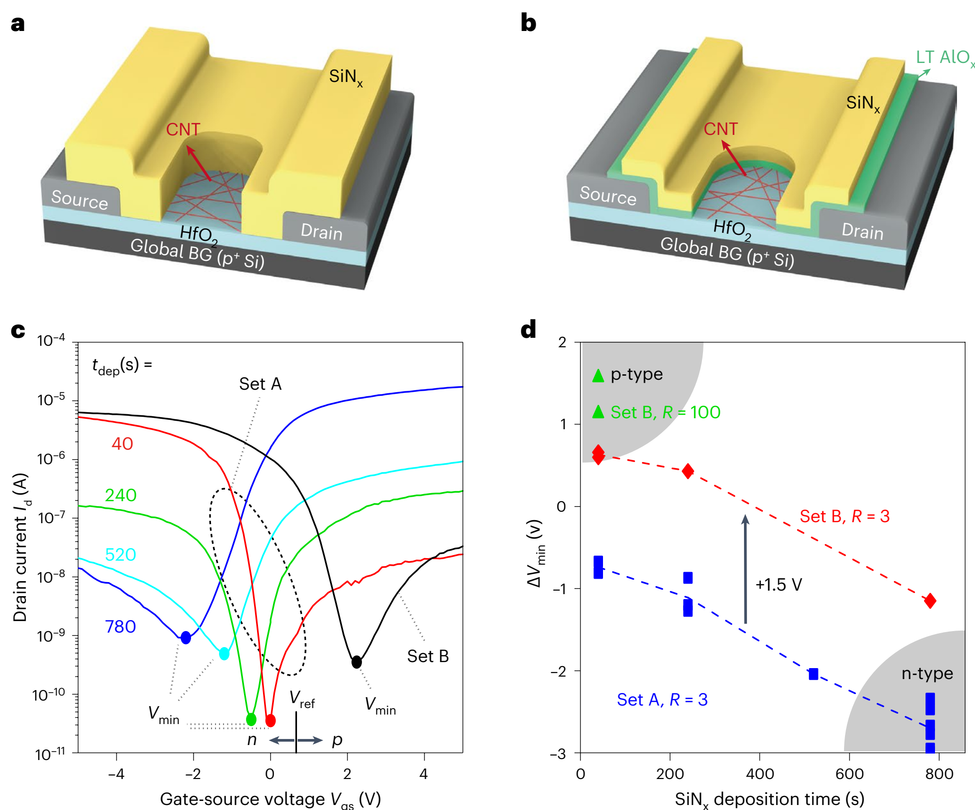

Fig. 4 | Development of solid-state extension doping. a, Cross-section schematic of a back-gate CNT FET used to develop n-type solid-state doping. **b**, Cross-section schematic of a BG CNT FET used to develop p-type solid-state doping. In both **a** and **b**, the opening in the dielectric layer is for illustration purposes only to reveal the CNT network. **c**, I_d versus V_{gs} curves (V_{ds} = 0.05 V) for single SiN_x films of different deposition time t_{dep} and R = 3 for n-type doping (set A, SiN_x t_{dep} as parameter) and for a SiN_x/LT AlO_x bilayer (set B) with R = 100 for SiN_x for p-type doping. **d**, Summary of experimentally obtained ΔV_{min} as a function of SiN_x deposition time t_{dep} for both single SiN_x films (set A) and SiN_x–LT AlO_x bilayers (set B, R = 3, 100). The ΔV_{min} curve for bilayers (R = 3) is shifted against the single layer SiN_x by +1.5 V along the ΔV_{min} axis, indicating the presence of an electrostatic dipole at the SiN_x–LT AlO_x interface. The preferred corners for n- and p-type doping are indicated. The lines are a guide to the eye only.

were proposed. Because Al–O–Si bonds have similar polarity at SiN_x–Al_2O_3 and SiO_2–Al_2O_3 interfaces, the latter model can explain our observation of a dipole at the SiN_x–Al_2O_3 interface. Although dipole layers are also reported at HfO_2–Al_2O_3 interfaces[46], the doping efficiency of such a dipole is less because of this interface and its corresponding dipole being located between the CNTs; this is in contrast to the SiN_x–Al_2O_3 interface, where the dipole is situated perpendicular to the CNT surface and surrounds the CNT to a large extent. The observation of n- and p-type MOSFET V_T being essentially symmetric to zero also excludes any effect due to a dipole at the HfO_2–Al_2O_3 interface and the assumption of a noticeable charge in the LT AlO_x layer because both polarity devices share the HfO_2–Al_2O_3 interface and the LT AlO_x layer in the gate region.

Thus, doping is found to be tunable with the presented techniques. The preferred corners for n- and p-type doping are located in the lower-right and upper-left areas, as indicated in Fig. 4d. Consequently, single SiN_x films with deposition time exceeding 650 s (R = 3) and SiN_x–LT AlO_x (SiN_x: 5 nm, R = 100; AlO_x: 1.5 nm) bilayers are selected for localized n- and p-type extension doping of our top-gate and complementary CNT MOSFETs, respectively.

Beyond the experimental observation of n- and p-type doping tunability, a deeper understanding of the physical mechanism behind doping by means of spatial charge transfer from localized defect levels in dielectrics is required to extract physical parameters, optimize such techniques and understand their limitations. In the past, the effect of spatial charge transfer from dielectrics has often been ascribed to a fixed charge uniformly distributed throughout the depth of the dielectric layer. Such models are simplistic and do not consider that each charge is associated with an energy level in the energy band structure of a solid. In the case of SiN_x, the defect structure is complex[47,48].

For illustration purposes, we use here the well-known Si dangling bond centre $\equiv Si^0$ termed K^0 (ref. 48). The K^0 centre is amphoteric, having a lower donor type transition level +/0 and a higher acceptor type transition level 0/−. A tight-binding recursion method[49] placed the +/0 transition level at −4.3 eV (ref. 50), which is essentially identical to the conduction band minimum E_c of the CNTs considered here. Calculated energy-band parameters have often been afflicted with substantial uncertainty; for the purpose of this treatise, we assume that the energy E_D of the +/0 transition level is situated 0.6 eV above the E_c of the CNT (ΔE = 0.6 eV). Note that for electron donation, the energy E_D of the SiN_x donor level must be located above E_c of the CNT channel. The density N_K^+ of ionized K^0 centres follows Fermi–Dirac statistics

$$N_K^+ = N_K^0 \left[1 - \frac{1}{1 + e^{\frac{E_D - E_F}{kT}}}\right]$$

where N_K^0, k, T are the density of K^0 defect centres, the Boltzmann constant and the absolute temperature, respectively. Solving Poisson's equation

$$\nabla(\kappa\nabla\varphi) = -\frac{\rho(\varphi)}{\varepsilon_0} = -\frac{q}{\varepsilon_0}\left\{N_K^+(\varphi) + p(\varphi) - n(\varphi)\right\}$$

using TCAD[40,51], where φ, ρ, and ε_0 are the electrostatic potential, the volume charge density, and the permittivity of vacuum, respectively,

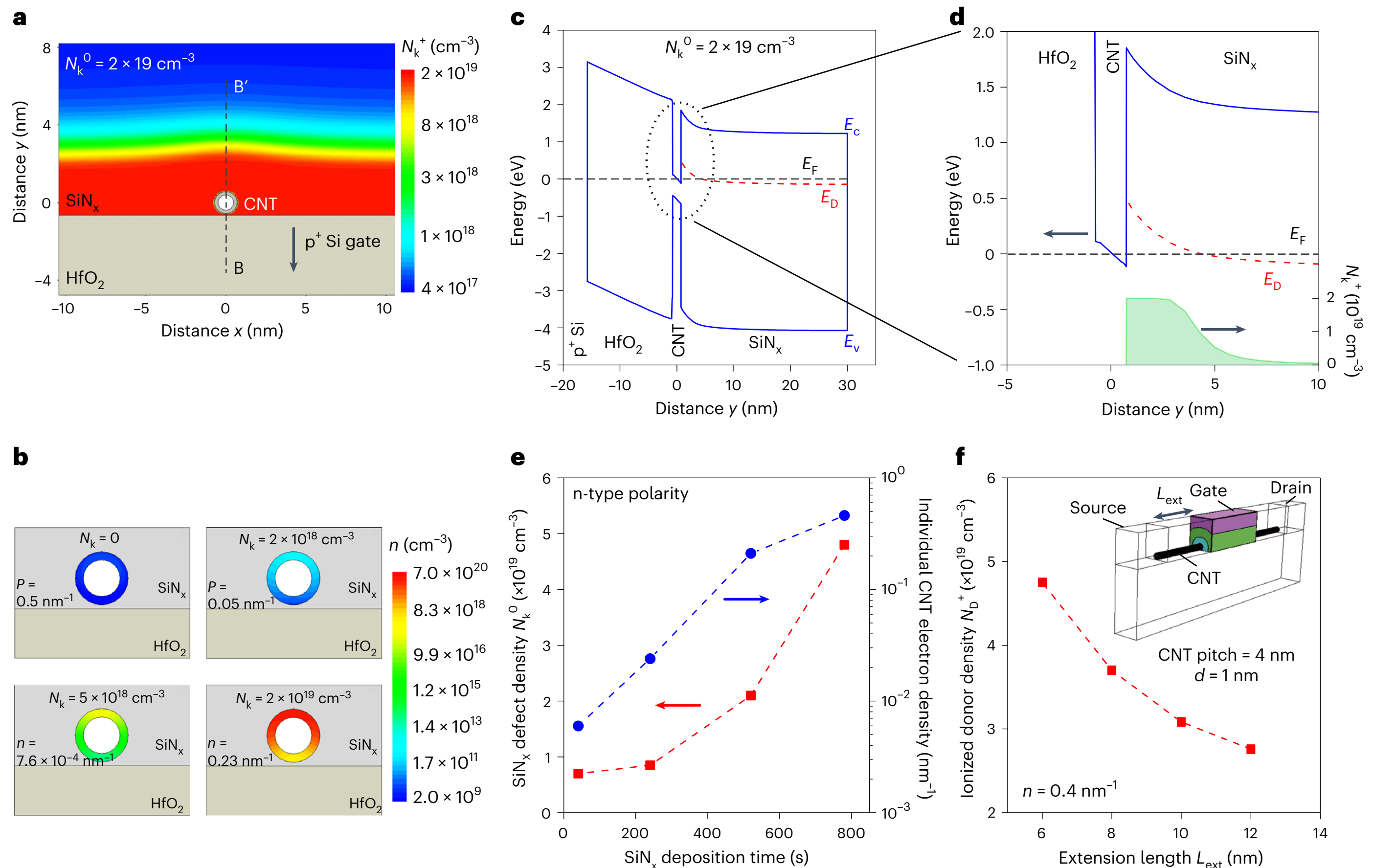

Fig. 5 | Modelling of solid-state extension doping. **a**, 2D density distribution of ionized K^0 defect centres N_K^+ for a cross-section perpendicular to the source-drain path in Fig. 4a. The SiN_x N_{K0} centre density and energy position ΔE of the +/0 level used in the simulations are uniform throughout the SiN_x film and equal to $N_{K0} = 2 \times 10^{19}$ cm^{-3} and $\Delta E = 0.6$ eV, respectively. The ionized charge N_K^+ originating from the SiN_x K^0 centres is confined to the vicinity of the CNT and the first few nanometres of the SiN_x layer. **b**, CNT carrier concentration distributions and electron and hole concentrations per unit length for SiN_x K^0 centre density ranging from 0 to 2×10^{19} cm^{-3}. **c**, Energy-band diagram for identical parameters along the line B–B′ shown in **a**. The work function of the p$^+$ Si substrate and the CNT diameter are 5.17 eV and 1.45 nm, respectively. **d**, Detail of energy-band diagram in **c** including ionized defect centre density N_K^+. **e**, SiN_x defect density N_{K0} and electron density n of individual CNTs as function of SiN_x deposition time. **f**, Calculated ionized donor density N_D^+ versus extension length L_{ext} required to maintain a CNT electron density n in the extension of 0.4 nm^{-1} for a potential future scaled planar device architecture, as shown in the inset. Here, ionized donors of concentration N_D^+ are assumed to be uniformly distributed in the extension volume with length L_{ext} and thickness of 5 nm.

we obtain the two-dimensional (2D) density distribution of ionized K^0 centres (N_K^+) shown in Fig. 5a for a cross-section perpendicular to the source-drain path of the device shown in Fig. 4a. The depth of the space charge region along the y axis can be estimated as

$$d \cong \sqrt{2\kappa\varepsilon_0 \Delta E / q N_K^0} = 4.5\,\text{nm}$$

using the parameters given in Fig. 5 and a κ value of 6 for SiN_x.

In the vicinity of the CNT, electron transfer from K^0 centres to the CNT is energetically favoured, leading to simultaneous n-type doping of the CNT (Fig. 5b) and K^0 centre ionization (Fig. 5a). For $N_{K0} = 0$, CNT polarity is p-type because of the work function (5.17 eV) of the p$^+$ Si back gate; however, CNT polarity is increasingly converted to n-type with higher N_{K0} density (Fig. 5b). Figure 5c shows the energy-band diagram along the line B–B′ in Fig. 5a. SiN_x energy bands are flat, and space charge is essentially zero beyond a SiN_x depth d of 5 nm. This is further illustrated in Fig. 5d, which shows a detail of the energy-band diagram in Fig. 5c including ionized defect centre density N_K^+. To finally close the loop between the experimentally extracted values of V_{min} for the investigated SiN_x deposition conditions (Fig. 4c) and the models developed above, the SiN_x defect density N_{K0} and the CNT carrier density are extracted for different SiN_x deposition times (Fig. 5e). This is accomplished by finding the density N_{K0} for each V_{min} shown in Fig. 4c and then calculating the hole and electron density (Fig. 5b) at zero bias using the identified N_{K0} values. Thus the SiN_x defect parameters are determined from electrical measurements. Figure 5f shows the calculated ionized donor density N_D^+ versus extension length L_{ext} required to maintain a CNT electron density n of 0.4 nm^{-1} for a potential future scaled device architecture, as shown in the inset, as calculated from electrostatic models[39] and the CNT density of states[40]. Our experimentally obtained N_{K0} values approach required values for extension doping of such scaled devices. To compromise between performance and leakage, we use 0.4 nm^{-1} as a doping strength. This target allows us to meet contact resistance requirements, especially for short contact length[2]; source-to-drain direct tunnelling, which increases with higher extension doping, meets targets as well.

Doping due to spatial charge transfer also has limitations, as implied in Fig. 5f, because the electrostatic potential generated from ionized dopants is relatively inefficient to induce charge carriers in a CNT near contact and gate-metal interfaces because of charge screening. Thus, doping CNTs at short extension length and CNT pitch is even more challenging. Limitations due to metal screening apply to all spatial charge-transfer techniques; for example, using extension gates

to induce electrostatic potential throughout a short region between source/drain (S/D) and gate metal is even less efficient and, further, not applicable to stacked nanosheets such as reported for 2D stacked nanosheet MOSFETs[52]. Another approach is substitutional doping; however, even assuming the absence of physical damage to the CNT, theory shows stronger Coulomb scattering for substitutional doping compared to spatial charge-transfer doping leading to more severe performance degradation of CNFETs[53], and strong device variations may result from random substitutional doping effects in a small volume. Spatial charge transfer from dielectrics for extension doping is also a critical component for future stacked 2D nanosheet devices[52]. 2D nanosheet MOSFETs require a vertically stacked architecture to meet IRDS requirements[15]. A promising approach is to provide extension doping by inner spacer dielectrics.

Conclusions

We have reported process modules for CNT MOSFET architecture fabrication with 2031 IRDS targets in mind. These modules could potentially be used to build a future, foundry-relevant CNT CMOS technology. We fabricated top-gate complementary CNT MOSFETs for which the devices' polarity is set and performance matching is accomplished exclusively by localized conformal solid-state extension doping, a module that is compatible with CMOS foundry resources. Localization of doping to extensions only is an important aspect of this approach and reduces device-to-device variability in a short-channel device as dopant fluctuations are a substantial source of variability. Enabled by the extension doping module, we provided impedance-voltage measurements and the extraction of interface state density D_{it} as a function of gap energy. The location of interface states in energy space is essential to support identification of their structural origin and develop feasible future passivation schemes.

Methods

Purification of semiconducting CNTs

Semiconducting CNTs are purified using a 1:1 ratio by weight of arc-discharge CNT powder (Carbon Solution, Inc., AP-CNT) and conjugated polymer PCz (poly[9-(1-octylonoyl)-9H-carbazole-2,7-diyl]) (American Dye Source, Inc.), which are dispersed at a concentration of 2 mg per ml in toluene. This mixture is sonicated with a tip sonicator (Sonic, VCX-750, 7 mm probe tip) for 30 min at 600 W in a 20 °C cool flowing water bath to dissipate excess heat. The dispersed solution is centrifuged in a swing bucket rotor (Beckman, Optima XPN-90, SW 32 Ti Swinging Bucket Rotor) at 50,000*g* for 20 min to remove the undispersed material. The top 90% of the supernatant is collected. Then the centrifugation process is repeated at 50,000*g* for 2 hours to further remove the metallic CNT. Finally, the top 90% supernatant is collected for the CNT network deposition by the immersion method.

CNT network deposition

CNT networks were deposited by the immersion method. The target substrates were immersed in the diluted CNT in toluene solution for 18 hours to form randomly orientated, uniform high-density CNT networks. After the deposition, the target substrate was soaked in toluene for 20 min and baking in ambient at 180 °C for 30 min.

Fabrication process of network CNT-based transistors

A 500 µm thick p^+-doped Si wafer (University Wafer no. 785) was used as the substrate for the back-gate FET devices for doping development, and a 500 µm high-resistivity Si wafer (University Wafer no. 3328) was used as the substrate for the complementary MOSFET devices. To remove unwanted impurities, Radio Corporation of America treatment was done, followed by a spin–rinse–dry cycle. A 20 nm HfO_2 film was deposited on the wafer at 200 °C using an ALD system (Fiji F202 Cambridge Nanotech) followed by CNT network deposition. The uniformity of the network CNTs across the entire wafer was confirmed by SEM (FEI Apreo). The density of the network CNTs and length distribution were verified by atomic force microscopy (VEECO Dimension 3100). The diameter distribution of the CNTs was extracted using TEM (Supplementary Fig. 3). The source and drain metal contact were defined by photolithography (Heidelberg MLA 150), and 30 nm Pd was deposited by e-beam evaporation (Temescal BJD 1800). The channel regions were protected by photoresist that was defined by photolithography, after which the excess CNTs (CNTs outside the FET structure) were removed by oxygen plasma etch (Oxford PlasmaLab 80). Subsequently, the residual photoresist on the channel region was removed using AZ NMP. The wafer was then diced, and the next steps were done on small chips.

Back-gate CNT FET for doping study

After the residual photoresist was removed with AZ NMP, SiN_x thin films were deposited using plasma-enhanced chemical vapor deposition (PECVD; Oxford PlasmaLab 80plus). Various thicknesses of SiN_x were deposited on top of the substrate by changing the deposition time. During all runs with different SiN_x deposition times, the system was kept at a temperature of 270 °C, and plasma was run at a frequency of 13.56 MHz at 20 W. The pressure of the chamber was kept at 900 mTorr with, for example, 5% SiH_4 (dilute in He) at a flow rate of 200 sccm and a NH_3 flow rate of 30 sccm ($R = 3$). To open the contacts, openings were defined by photolithography and SiN_x etched using buffered oxide etchant (BOE). The detailed fabrication flow of the back-gate FETs is shown in Supplementary Fig. 5.

Top-gate CNT n-MOSFET

The chip with predefined source and drain contacts was first baked at 180 °C for 5 mins to remove moisture. Afterwards, 100 nm SiN_x ($R = 3$) was deposited using the PECVD tool. To deposit the gate oxide for the gate region, the SiN_x in the gate region was removed using wet-etch methods. The gate region was defined by photolithography and the SiN_x etched with BOE. Subsequently, the entire chip was immersed in AZ NMP overnight to remove all photoresist. A LT AlO_x film with a thickness of 1.5 nm was deposited by ALD at 50 °C followed by an additional 4 nm high-temperature Al_2O_3 that was also deposited by ALD but at 250 °C. To deposit the top gate, the pattern was defined by photolithography and 30 nm Pd was deposited by e-beam evaporation. Vias over contact pads were patterned by lithography, and then SiN_x and gate dielectrics were etched with BOE to enable electrical measurements. The detailed MOSFET process flow is shown in Supplementary Fig. 6.

Top-gate CNT p-MOSFET

The chip with predefined source and drain contacts was first baked at 180 °C for 5 mins to avoid any moisture from the previous process. A 1.5 nm LT AlO_x film was deposited on top of the chip by ALD at 50 °C. Then an additional 4 nm Al_2O_3 were deposited by ALD at 250 °C. Similar to the n-MOSFET top-gate process, the gate region was defined by photolithography and the 30 nm Pd gate metal was deposited by e-beam evaporation. Next, 5 nm of SiN_x ($R = 100$) was deposited using the PECVD tool. To perform the electrical measurement, openings on contact pads were made by photolithography and BOE etch.

I–*V* measurement

All the transistor characterization measurements were performed in a common-source configuration. Electrical *I*–*V* data was measured using a shielded probe station and an Agilent B1500A semiconductor device parameter analyzer equipped with high-resolution source monitor units. The transfer characteristics (I_d–V_{gs}) were performed at a bias sweep rate of 120 mV s^{-1} with steps of 30 mV. For the output characteristics (I_d–V_{ds}), the drain voltage (V_{ds}) was swept from 0 to +1 V or −1 V for n-MOSFET and p-MOSFET, respectively, in steps of 20 mV and at a sweep rate of 100 mV s^{-1}. The gate-source voltage V_{gs} was swept from the off state of the device ($V_{gs} = -0.5$ V to 2 V for n-MOSFET and $V_{gs} = 0.5$ V to −2 V for p-MOSFET). The back-gate FET transfer characteristics were combined from two different V_{gs} sweeps. In each sweep, V_{gs} was varied

either from 0 to +5 V or from 0 to −5 V in steps of 100 mV at a sweep rate of 400 mV/s. This technique was used to minimize the effect of charge trapping at a large-gate bias of up to 5 V, which can lead to shift of the I_d–V_{gs} curve along the V_{gs} axis.

C–*V* measurement

Multifrequency *C*–*V* and *G*–*V* measurements were carried out using a precision LCR metre (Agilent 4284A) connected to a Keithley 2420. The 'high' terminal was connected to both source and drain and the 'low' terminal to the gate. A small-signal ac excitation with amplitude of 25 mV was applied to the device, and the d.c. bias was swept with a rate of 12 mV s^{-1} in steps of 30 mV. An external bias (Keithley 2420) was connected to the LCR metre using an adaptor (Keysight 16065C) to control the bias applied to the sample. Simultaneous multifrequency sweeps were performed by sweeping the bias and obtaining the capacitance at three different frequencies at each bias point. The device was encapsulated in a Faraday cage to cancel out any noise from the environment. Before any measurements, the parasitic capacitances were cancelled out by performing an open-and short calibration on fabricated on-chip open-and-short de-embedding structures. All devices were measured at three different frequencies: 1 MHz, 500 kHz and 100 kHz.

TCAD simulations

Electrostatic models are implemented in either Nano Device Simulator[39] or Sentaurus Device framework[51]. An analytical CNT density-of-state model depending on CNT diameter is used to compute the carrier density in the CNT[40].

For the simulations supporting Fig. 3, the number of CNTs under the gate *N* is estimated from the accumulation capacitance as follows:

$$N = \frac{C_{\rm exp}}{C'_{\rm mod} L_{\rm av}} = \frac{C_{\rm exp}}{C'_{\rm mod} \left(L_{\rm g} / \cos \varphi\right)}$$

where $C_{\rm exp}$, $C'_{\rm mod}$, $L_{\rm av}$ and φ are the total measured accumulation capacitance, the calculated average accumulation capacitance per CNT unit length and the average length and average orientation of CNTs under the gate, respectively, with $L_{\rm av} = L_{\rm g} / \cos \varphi$. $C'_{\rm mod} = 1.31 \times 10^{-10}$ F m^{-1} is obtained using the Poisson solver in the Nano Device Simulator[39] and the CNT density-of-state model[40] for the geometry of the gate-stack cross-section in Fig. 2 (5.5 nm Al_2O_3 with $k = 7.8$ (ref. 9)). The corresponding oxide capacitance per unit length is 1.65×10^{-10} F m^{-1}. Assuming an average orientation of 45°, $N_n = 4{,}966$ and $N_p = 4{,}048$ are obtained. Note that the quantities extracted for individual CNTs including carrier density n or p $(= Q/(NL_{\rm av}q)$, normalized interface state parallel conductance $G_{\rm p}/(\omega q N L_{\rm av})$ and interface state density $D_{\rm it} = 2.4 G_{\rm p,peak}/(\omega q N L_{\rm av})$ do not depend on the assumption of average CNT orientation φ because $NL_{\rm av} = C_{\rm exp}/C'_{\rm mod}$, which is independent of φ. Here, $G_{\rm p,peak}$ is the peak value of the $G_{\rm p}$ versus $V_{\rm g}$ dependence.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

1. Cao, Q., Tersoff, J., Farmer, D. B., Zhu, Y. & Han, S. J. Carbon nanotube transistors scaled to a 40-nanometer footprint. *Science* **356**, 1369–1372 (2017).
2. Su, S. K. et al. Perspective on low-dimensional channel materials for extremely scaled CMOS. In *2022 Symposium on VLSI Technology and Circuits*, *Digest of Technical Papers*, 403–404 (IEEE, 2022).
3. Xu, L., Qiu, C., Zhao, C., Zhang, Z. & Peng, L. M. Insight into ballisticity of room-temperature carrier transport in carbon nanotube field-effect transistors. *IEEE Trans. Electron Devices* **66**, 3535–3540 (2019).
4. Zhou, X., Park, J. Y., Huang, S., Liu, J. & McEuen, P. L. Band structure, phonon scattering, and the performance limit of single-walled carbon nanotube transistors. *Phys. Rev. Lett.* **95**, 146805 (2005).
5. Gilardi, C. et al. Extended scale length theory targeting low-dimensional FETs for carbon nanotube FET digital logic design-technology co-optimization. In *Technical Digest—International Electron Devices Meeting*, 27.3.1–27.3.4 (IEEE, 2021).
6. Hills, G. et al. Understanding energy efficiency benefits of carbon nanotube field-effect transistors for digital VLSI. *IEEE Trans. Nanotechnol.* **17**, 1259–1269 (2018).
7. Cao, Q. & Han, S. J. Single-walled carbon nanotubes for high-performance electronics. *Nanoscale* **5**, 8852–8863 (2013).
8. Pitner, G. et al. Low-temperature side contact to carbon nanotube transistors: resistance distributions down to 10 nm contact length. *Nano Lett.* **19**, 1083–1089 (2019).
9. Pitner, G. et al. Sub-0.5 nm interfacial dielectric enables superior electrostatics: 65 mV/dec top-gated carbon nanotube FETs at 15 nm gate length. In *Technical Digest—International Electron Devices Meeting*, 3.5.1–3.5.4 (IEEE, 2020).
10. Liu, L. et al. Aligned, high-density semiconducting carbon nanotube arrays for high-performance electronics. *Science* **368**, 850–856 (2020).
11. Sun, W. et al. Precise pitch-scaling of carbon nanotube arrays within three-dimensional DNA nanotrenches. *Science* **368**, 874–877 (2020).
12. Lin, Y. et al. Scaling aligned carbon nanotube transistors to a sub-10 nm node. *Nat. Electron.* **6**, 506–515 (2023).
13. Liu, C. et al. Complementary transistors based on aligned semiconducting carbon nanotube arrays. *ACS Nano* **16**, 21482–21490 (2022).
14. Chao, T. A., Pitner, G., Wong, H.-S. P., Wang, H. & Chang, W. H. Small molecular additives to suppress bundling in dimensional limited self-alignment method for high-density aligned CNT arrays. In *22nd International Conference on the Science and Applications of Nanotubes and Low-Dimensional Materials*, Parallel Symposia on Low Dimensional Electronics (NT22, 2022).
15. *International Roadmap for Devices and Systems, More Moore* (IEEE, 2022); https://irds.ieee.org/images/files/pdf/2022/2022IRDS_MM.pdf
16. Lin, Q. et al. Bandgap extraction at 10 K to enable leakage control in carbon nanotube MOSFETs. *IEEE Electron Device Lett.* **43**, 490–493 (2022).
17. Wong, H.-S. Beyond the conventional transistor. *IBM J. Res. Dev.* **46**, 133–168 (2002).
18. *International Roadmap for Devices and Systems, Lithography* (IEEE, 2022); https://irds.ieee.org/editions/2022
19. Su, S. K. et al. Impact of metal hybridization on contact resistance and leakage current of carbon nanotube transistors. *IEEE Electron Device Lett.* **43**, 1367–1370 (2022).
20. Zhang, Y., Zhang, J. & Su, D. S. Substitutional doping of carbon nanotubes with heteroatoms and their chemical applications. *ChemSusChem* **7**, 1240–1250 (2014).
21. Javey, A. et al. High performance n-type carbon nanotube field-effect transistors with chemically doped contacts. *Nano Lett.* **5**, 345–348 (2005).
22. Chen, J., Klinke, C., Afzali, A., Chan, K. & Avouris, P. Self-aligned carbon nanotube transistors with novel chemical doping. In *Technical Digest—International Electron Devices Meeting*, 695–698 (IEEE, 2004).
23. Kim, S. M. et al. Erratum: reduction-controlled viologen in bisolvent as an environmentally stable n-type dopant for carbon nanotubes (*J. Am. Chem. Soc.* (2009) 131(327–331)). *J. Am. Chem. Soc.* **131**, 5010 (2009).

24. Wang, C. et al. Device study, chemical doping, and logic circuits based on transferred aligned single-walled carbon nanotubes. *Appl. Phys. Lett.* **93**, 033101 (2008).
25. Franklin, A. D. & Chen, Z. Length scaling of carbon nanotube transistors. *Nat. Nanotechnol.* **5**, 858–862 (2010).
26. Srimani, T., Hills, G., Bishop, M. D. & Shulaker, M. M. 30-nm contacted gate pitch back-gate carbon nanotube FETs for sub-3-nm nodes. *IEEE Trans. Nanotechnol.* **18**, 132–138 (2019).
27. Qiu, C. et al. Scaling carbon nanotube complementary transistors to 5-nm gate lengths. *Science* **355**, 271–276 (2017).
28. Franklin, A. D. et al. Carbon nanotube complementary wrap-gate transistors. *Nano Lett.* **13**, 2490–2495 (2013).
29. Ha, T. J. et al. Highly uniform and stable n-type carbon nanotube transistors by using positively charged silicon nitride thin films. *Nano Lett.* **15**, 392–397 (2015).
30. Lau, C., Srimani, T., Bishop, M. D., Hills, G. & Shulaker, M. M. Tunable n-type doping of carbon nanotubes through engineered atomic layer deposition HfO_x films. *ACS Nano* **12**, 10924–10931 (2018).
31. Park, R. S. et al. Molybdenum oxide on carbon nanotube: doping stability and correlation with work function. *J. Appl. Phys.* **128**, 045111 (2020).
32. Ilani, S., Donev, L. A. K., Kindermann, M. & McEuen, P. L. Measurement of the quantum capacitance of interacting electrons in carbon nanotubes. *Nat. Phys.* **2**, 687–691 (2006).
33. Javey, A., Guo, J., Wang, Q., Lundstrom, M. & Dai, H. Ballistic carbon nanotube field-effect transistors. *Nature* **424**, 654–657 (2003).
34. Zhang, Z. et al. Sub-nanometer interfacial oxides on highly oriented pyrolytic graphite and carbon nanotubes enabled by lateral oxide growth. *ACS Appl. Mater. Interfaces* **14**, 11873–11882 (2022).
35. Shahrjerdi, D. et al. High-performance air-stable n-type carbon nanotube transistors with erbium contacts. *ACS Nano* **7**, 8303–8308 (2013).
36. Yang, L. et al. Efficient photovoltage multiplication in carbon nanotubes. *Nat. Photonics* **5**, 672–676 (2011).
37. Ding, L. et al. Y-contacted high-performance n-type single-walled carbon nanotube field-effect transistors: scaling and comparison with Sc-contacted devices. *Nano Lett.* **9**, 4209–4214 (2009).
38. Sze, S. M. *Physics of Semiconductor Devices* 2nd edn (Wiley, 1981).
39. Stanojevic, Z. et al. Nano device simulator—a practical Subband-BTE solver for path-finding and DTCO. *IEEE Trans. Electron Devices* **68**, 5400–5406 (2021).
40. Zhao, Y., Liao, A. & Pop, E. Multiband mobility in semiconducting carbon nanotubes. *IEEE Electron Device Lett.* **30**, 1078–1081 (2009).
41. Nicollian, E. H. & Brews, J. R. *MOS (Metal Oxide Semiconductor) Physics and Technology*, 213–218 (Wiley, 1982).
42. Cao, Q. et al. Origins and characteristics of the threshold voltage variability of quasiballistic single-walled carbon nanotube field-effect transistors. *ACS Nano* **9**, 1936–1944 (2015).
43. Matsukawa, T. et al. Decomposition of on-current variability of NMOS FinFETs for prediction beyond 20 nm. *IEEE Trans. Electron Devices* **59**, 2003–2010 (2012).
44. Kamata, H. & Kita, K. Design of Al_2O_3/SiO_2 laminated stacks with multiple interface dipole layers to achieve large flatband voltage shifts of MOS capacitors. *Appl. Phys. Lett.* **110**, 102106 (2017).
45. Jakschik, S. et al. Dielectric backside passivation—improvements by dipole optimization. In *Proc. 26th European Photovoltaic Solar Energy Conference and Exhibition* (ed. Ossenbrink, H. A.) 2252–2255 (WIP Munich, 2011).
46. Zhang, Y., Choi, M., Wang, Z. & Choi, C. Dipole formation to modulate flatband voltage using ALD Al_2O_3 and La_2O_3 at the interface between HfO_2 and Si or Ge substrates. *Appl. Surf. Sci.* **609**, 155295 (2023).
47. Robertson, J. Defects and hydrogen in amorphous silicon nitride. *Philos. Mag. B* **69**, 307–326 (1994).
48. Di Valentin, C., Palma, G. & Pacchioni, G. Ab initio study of transition levels for intrinsic defects in silicon nitride. *J. Phys. Chem. C Nanomater. Interfaces* **115**, 561–569 (2011).
49. Robertson, J. Defect and impurity states in silicon nitride. *J. Appl. Phys.* **54**, 4490–4493 (1983).
50. Robertson, J. & Powell, M. J. Gap states in silicon nitride. *Appl. Phys. Lett.* **44**, 415–417 (1984).
51. *Sentaurus Device User Guide Version T-2022.03* (Synopsis, 2022).
52. Chung Y.-Y. et al. First demonstration of GAA monolayer-MoS_2 nanosheet nFET with 410μA/μm I_D at 1V V_D at 40nm gate length. In *Technical Digest—International Electron Devices Meeting*, 823–626 (IEEE, 2022).
53. Pitner G. et. al. Building high performance transistors on carbon nanotube channel. In *2023 Symposium on VLSI Technology and Circuits, Digest of Technical Papers*, T8-1 (IEEE, 2023).

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Author contributions

Z.Z. and M.P. contributed equally. Z.Z. conducted the device fabrication and measurement. M.P. developed the impedance and doping models, device layout and data analysis. G.P., W.E.S., N.S. and T-E.L. contributed to device fabrication, and S.N. supported impedance measurements. S.-K.S. and G.D. contributed to device modelling. T.-A.C. provided the CNT substrates. S.L.L., V.D.-H.H. and C.-F.H. provided TEM analysis. I.R., A.C.K., P.B. and H.-S.P.W. guided the project. Z.Z. and M.P. prepared the paper draft, and all the authors commented on the final version.

Competing interests

The authors declare no competing interests.

Additional information

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