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Band-to-Band Tunneling Leakage Current Characterization and Projection in Carbon Nanotube Transistors

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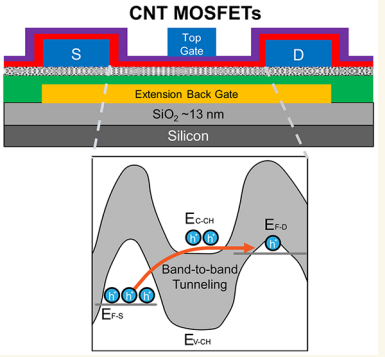
ABSTRACT: **Carbon nanotube (CNT) transistors demonstrate high mobility but also experience off-state leakage due to the small effective mass and band gap. The lower limit of off-current (I_{MIN}) was measured in electrostatically doped CNT metal-oxide-semiconductor field-effect transistors (MOSFETs) across a range of band gaps (0.37 to 1.19 eV), supply voltages (0.5 to 0.7 V), and extension doping levels (0.2 to 0.8 carriers/nm). A nonequilibrium Green's function (NEGF) model confirms the dependence of I_{MIN} on CNT band gap, supply voltage, and extension doping level. A leakage current design space across CNT band gap, supply voltage, and extension doping is projected based on the validated NEGF model for long-channel CNT MOSFETs to identify the appropriate device design choices. The optimal extension doping and CNT band gap design choice for a target off-current density are identified by including on-current projection in the leakage current design space. An extension doping level >0.5 carrier/nm is required for optimized on-current.**



KEYWORDS: *carbon nanotube, MOSFET, leakage current, band-to-band tunneling, band gap, supply voltage, extension doping*

Carbon nanotubes (CNTs) are promising candidates as channel materials for extremely scaled technology nodes.[1−6] Due to the CNT's naturally 1 nm thin body and high carrier mobility, CNT metal-oxide-semiconductor field-effect transistors (MOSFETs) are projected to achieve up to 7× energy-delay product (EDP) benefits compared to Si for beyond 2 nm technology nodes.[7] Moreover, the low-temperature fabrication of CNT MOSFETs (i.e., <400 °C) enables monolithic three-dimensional (3D) ultradense integration of logic and memory, leading to even larger energy and throughput benefits at the application level.[8−11]

Much progress has been made on CNT transistors (CNFETs), including a low contact resistance of 6.5 kΩ/CNT at 10 nm contact length for p-type and 5.1 kΩ/CNT at 20 nm contact length for n-type;[12,13] a high-density aligned CNT assembly from 250 to 500 CNTs/μm;[6,14−16] and an excellent short-channel effect immunity when reducing gate lengths down to 15 nm due to a 0.35 nm interfacial dielectric (k = 7.8) and a 2.5 nm high-k ALD dielectric (k = 24) top-gate stack.[17] Furthermore, VLSI CNT CMOS systems have already been demonstrated[18] and integrated into multiple Si facilities at mature nodes.[19−21] However, the small band gap (tunable from 0.6 to 1.1 eV for CNTs[13] vs 1.12 eV for Si) and the low effective mass of CNTs have potentially large drain leakage, which may increase the standby power and degrade the energy efficiency of CNT transistors.[22−24] Therefore, it is essential to understand how design choices, including the CNFET device structure, CNT diameter, supply voltage, and extension doping level, can be engineered to control the leakage current. For example, in our recent work, we have developed a method to extract CNT band gaps from CNT MOSFETs' electrical characteristics and analyzed the impact of CNT band gaps on the leakage current.[24]

In this paper, we present a systematic study that simultaneously captures the leakage current dependencies on device design parameters, which enables the optimization of an extremely scaled CNT MOSFET, given the multiple trade-offs that affect device performance and energy efficiency.[7] Specifically, this paper (1) measures the limits of the CNT MOSFET drain leakage current against a broader design space, including band gap, supply voltage, and extension doping levels; (2) explains the impact of various device structures on

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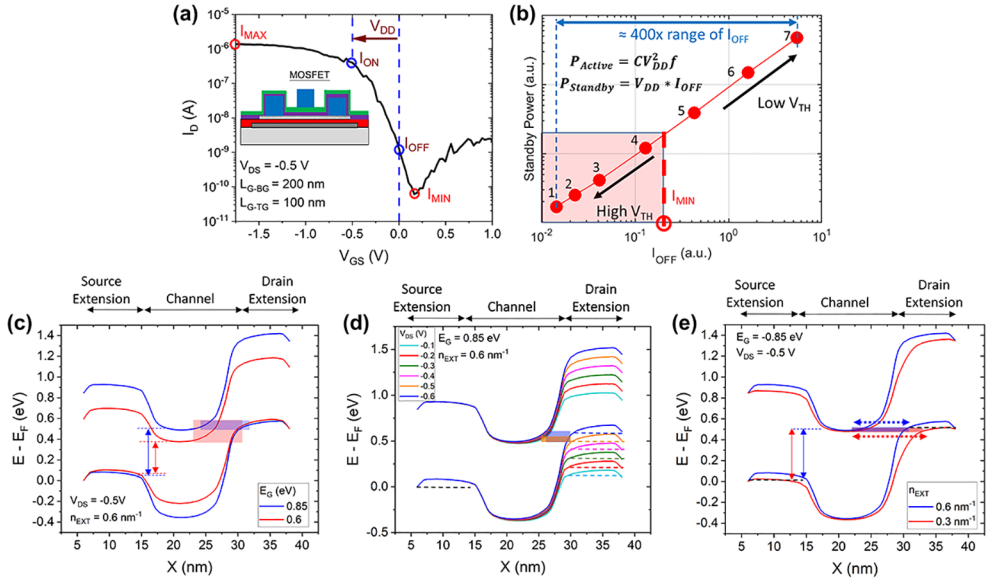

Figure 1. (a) Example I_D−V_{GS} for the single-CNT MOSFET. I_{ON} is indicated at $V_{GS} = V_{DS} = V_{DD}$. The I_{MIN} represents the point beyond which any V_{TH} increase does not result in standby power reduction. The I_{MAX} represents the largest I_D in the given V_{GS} sweeping range, as a simplified metric of transistor on-current without defining a V_{TH} or V_{DD}. (b) Transistor standby power versus off-current (I_{OFF}) in a log−log scale by tuning transistor threshold voltage (V_{TH}) from 5 nm node Si CMOS technology.[25] (c−e) Band diagrams generated by TCAD simulation[29] illustrate CNT MOSFET leakage sensitivity to (c) CNT band gap (E_G), (d) drain bias (V_{DS}), and (e) extension doping (n_{EXT}). The arrow on the source side indicates the energy transition required for source-to-channel BTBT. The highlighted region on the drain side indicates the energy range and the physical locations where BTBT may occur between the conduction band edge in channel $E_{C\text{-}CH}$ and unoccupied states below the Fermi level in the drain valence band $E_{F\text{-}D}$. At the same bias conditions, a smaller band gap has a larger BTBT due to both a smaller source-to-channel energy transition and larger energy overlap between channel $E_{C\text{-}CH}$ and drain $E_{F\text{-}D}$. Increasing the magnitude of V_{DS} similarly leads to larger energy overlap between channel E_C and drain $E_{F\text{-}D}$. Lower extension doping primarily increases the tunneling distance between channel and drain, suppressing BTBT.

the leakage current based on a single parameter, the tunneling distance; (3) projects the range of tunable off-current to identify the CNT MOSFETs' design space for digital logic platform technologies; and (4) identifies the best design choices to maximize on-current for a target off-current density.

RESULTS AND DISCUSSION

I. Understanding the Leakage Power Challenge in Carbon Nanotube MOSFETs. To understand fundamental limits of leakage power in CNT MOSFETs, we first must define the significance of I_{MIN} as it relates to I_{OFF}. Figure 1a shows the I_D−V_{GS} for a typical CNT MOSFET, labeling: (1) I_{OFF} at $V_{GS} = 0$ V, (2) I_{ON} at $V_{GS} = V_{DS} = V_{DD}$, (3) I_{MAX} at the largest $|V_{GS}|$, and (4) $I_{MIN} = \min(I_D)$. Figure 1b displays the linear relationship between standby power and I_{OFF} across a ∼400× range tuned by threshold voltage (V_{TH}) at a fixed V_{DD} for 5 nm node Si CMOS technology.[25] Both high-speed compute and low-energy system-on-chip applications utilize granular standard cell-level control over transistor leakage by selecting a high V_{TH} for noncritical path circuits (Figure 1a, points #1−4) and low V_{TH} (points #5−7) on critical paths to meet timing requirements. While I_{OFF} is influenced by V_{TH} and subthreshold swing, I_{MIN} is the key metric to evaluate the limit of energy efficiency, as no change in V_{TH} can further reduce the off-current.

Next, we define the dominant leakage mechanism that determines I_{MIN} in CNT MOSFETs. Contributions to drain current at I_{MIN} may include thermionic emission, gate leakage, source-drain tunneling (SDT), band-to-band tunneling (BTBT), and Schottky tunneling (Figure S1a). The gate leakage of CNFETs is minimized based on the recent improvements in the top-gate stack[17] and thus is a negligible contribution to total leakage in this study (Figure S1b). For CNT MOSFETs in this work with gate length >20 nm, nonequilibrium Green's function (NEGF) models predict that SDT is negligible; however, this effect will be important to study in future work using shorter gate lengths.[24] Similar to SDT, Schottky tunneling in MOSFETs is negligible for L_{EXT} > 20 nm.[5] Hence, I_{MIN} is determined by the BTBT leakage current in long-channel CNT MOSFETs with long extensions. Figure S1c,d and Table S1 compare three CNFET structures studied previously in the literature, which have different dominant leakage mechanisms: Schottky-barrier field-effect transistor (SBFET), asymmetric-SBFET (a-SBFET), and MOSFET. While SBFETs are easier to fabricate in academic research facilities, most modern scaled logic devices have a MOSFET structure with a spacer region between the source/drain contacts and the gate to reduce parasitic capacitance.[26−28] Therefore, this work focuses on studying the factors that influence BTBT in CNT MOSFETs.

The band diagrams generated by technology computer-aided design (TCAD)[29] in Figure 1c−e explain how BTBT is influenced by design parameters including (1) channel material band gap (E_G), (2) supply voltage (V_{DD}), and (3) extension doping (n_{EXT}). It is unique to CNFETs that the channel material band gap is tunable with a wide range from 0.6 to 1.1 eV as the CNT band gap depends on the diameter.[13] Table S1 summarizes previous literature that measures CNFETs' off-current considering only one of these parameters,[22−24,30−36] while this work simultaneously captures all three effects. Understanding the BTBT mechanism and calibrating device

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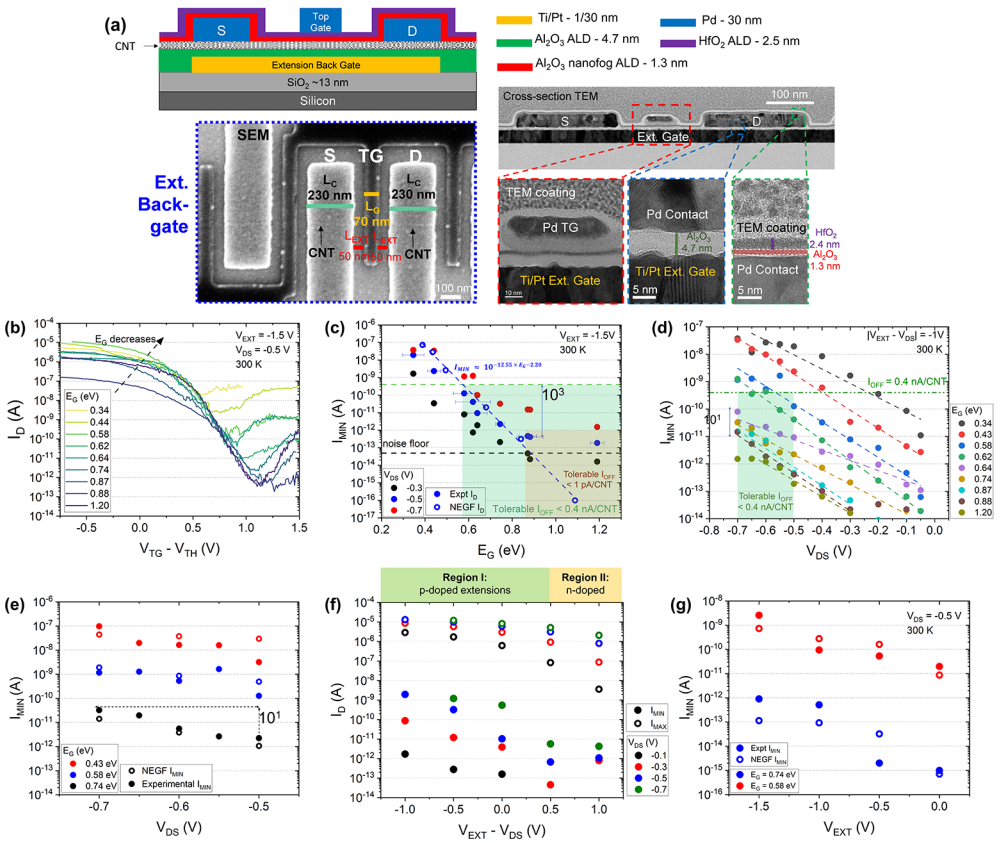

Figure 2. Single-CNT MOSFET device structure. (a) Cross-sectional schematic, top-down SEM image, and cross-sectional TEM images of a typical device after fabrication. Low-temperature atomic layer deposition (ALD) is used to deposit the 1.3 nm interfacial Al_2O_3.[17] All devices in this work have the same dimensions. (b) I_D−V_{GS} at 300 K for nine CNFETs with E_G = from 0.34 to 1.20 eV at −0.5 V V_{DS}. The V_{TH} is shifted to set I_{OFF}. (c) Experimental I_{MIN} at 300 K versus E_G extracted for nine single-CNT top-gate MOSFETs for V_{DS} = −0.3, −0.5, and −0.7 V, showing good agreement with NEGF-simulated I_{MIN}. The I_{MIN} increases by ∼3 orders of magnitude as E_G increases from 0.58 eV (∼1.46 nm CNT diameter) to 0.87 eV (∼1.1 nm CNT diameter). Error bars indicate the uncertainty in the extracted band gap accounting for the margin of error in the fitted slope, *y*-intercept, as well as the averaging effect from two to three repeated measurements. (d) I_{MIN} at 300 K versus V_{DS} for the nine single-CNT top-gate MOSFETs with E_G between 0.34 to 1.20 eV. The I_{MIN} increases by ∼1.2 orders of magnitude as V_{DS} decreases from −0.5 to −0.7 V. The dashed lines are the linear regression lines of log(I_{MIN}) versus V_{DS} with an average slope of −6.05. We notice the slope of log(I_{MIN}) − V_{DS} should be considered only in the low-bias regime for a small CNT band gap. Indeed, when V_{DS} > E_G, I_{MIN} is expected to saturate[41,42] (e.g., for E_G = 0.34 and 0.58 eV; the absence of saturation for E_G = 0.43 eV can be attributed to data variability). (e) Comparison of NEGF-simulated and experimental I_{MIN} versus V_{DS} for CNT MOSFETs at E_G = 0.43, 0.58, and 0.74 eV, showing reasonable agreement. (f) I_{MIN} and I_{MAX} at 300 K versus $|V_{EXT} - V_{DS}|$ for the same device in Figure S4b. The drain extension doping level remains constant at a given $V_{EXT} - V_{DS}$ for all drain bias. The I_{MIN} has a similar trend against $|V_{EXT} - V_{DS}|$ for all four V_{DS}. (g) The NEGF-simulated (hollow circles) and experimental I_{MIN} (solid circles) at 300 K for E_G = 0.58 eV (red) and 0.74 eV (blue) in single-CNT MOSFETs with a bottom extension gate, showing reasonable agreement.

leakage models is a key milestone to enable design-technology-co-optimization (DTCO) of CNT MOSFETs for different target applications.

II. CNT MOSFET Device Structure. P-type MOSFETs with single-CNT channels were fabricated as described in Figure S2 on CVD-grown aligned CNTs with a broad diameter distribution.[37] As shown in the cross-sectional schematic in Figure 2a, a top-gate electrode modulates the channel potential, and an overlapping bottom-gate extension electrode allows us to conveniently modulate the doping level in the extensions during measurement. In practical device technology, solid-state doping will be used instead of the extension gate.[13,38] The scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images in Figure 2a verify the single-CNT channel and label all key dimensions, including the gate length (L_G) of 70 nm and extension length (L_{EXT}) of 50 nm used in this paper.

III. CNT MOSFET Leakage Data and Discussion. *a. I_{MIN} Dependence on E_G, V_{DS}, and n_{EXT}.* To better understand how BTBT depends on the band gap, we used a band gap extraction method that we developed in our previous work[24] (summarized in Figure S3) on nine single-CNT p-type MOSFETs, with CNT band gap ranging from 0.35 ± 0.05 eV to 1.19 ± 0.05 eV. The I_D−V_{TG} of nine single-CNT MOSFETs was measured at 300 K while stepping V_{DS} at a constant $|V_{EXT} - V_{DS}|$ (Figure S4a) or stepping the extension gate bias (V_{EXT}) at a given V_{DS} to change the n_{EXT} (Figure S4b), which maintains the same drain n_{EXT} at different V_{DS}. This constant drain extension doping is essential to decoupling the effects of V_{DS} and n_{EXT} on BTBT at the channel-drain junction.

Figure 2b,c shows that the I_{MIN} decreases exponentially from 20 nA/CNT to sub-1 pA/CNT as E_G increases from 0.35 to 0.88 eV at −0.5 V V_{DS}. Therefore, considering a CNT density

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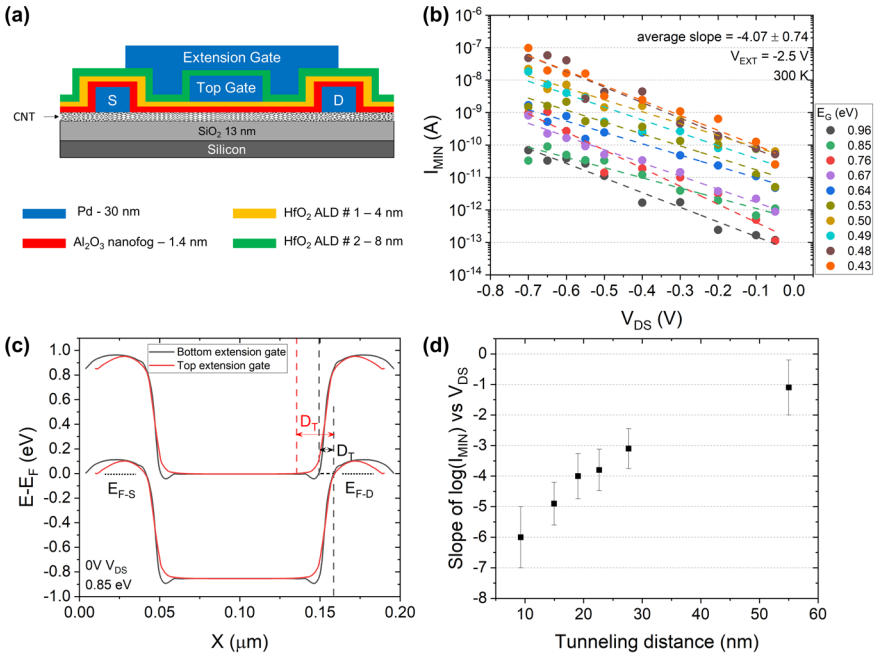

Figure 3. (a) Device structure of the CNT MOSFETs with a top extension gate. A top-gate electrode modulates the channel potential, and an overlapping top-gate extension electrode is used to modulate the doping level in the extension. (b) I_{MIN} at 300 K versus V_{DS} for the 10 single-CNT top-gate MOSFETs with device structure shown in (a) and E_G between 0.43 to 0.96 eV at degenerate doping level. The I_{MIN} increases <1 order of magnitude as V_{DS} decreases from −0.5 to −0.7 V. Compared with a bottom extension gate as shown in Figure 2a, a top extension gate structure shows a smaller linear regression slope of log(I_{MIN}) versus V_{DS}. (c) A TCAD-generated band diagram for the CNT MOSFET with a bottom extension gate (black) and top extension gate (red) at 0 V V_{DS}. The Fermi level of the source and drain extensions ($E_{F\text{-}S}$ and $E_{F\text{-}D}$), labeled by the dotted lines, are located near the bottom of the valence band as the extensions are degenerately doped. The tunneling distance (D_T), labeled by the solid arrows between dashed lines, is defined as the distance which the holes travel from the channel conduction band edge to drain extension valence band edge at V_{DS} = 0 V. (d) The average linear regression slope of experimentally measured log(I_{MIN}) versus simulation-extracted tunneling distances for six different device structures summarized in Table S2. The error bars represent the standard deviation of the slope extracted from a range of E_G.

of 250 CNTs/μm, a high-performance I_{OFF} density target of 100 nA/μm can be achieved with $E_G \geq 0.58$ eV; and a low-power target of 250 pA/μm can be met with $E_G \geq 0.88$ eV. A NEGF model simulates inelastic BTBT assisted by optical phonons based on the same device structure in Figure 2a with similar band gaps to the extracted values as inputs.[39,40] Importantly, the inclusion of inelastic scattering mechanisms (such as emission of optical phonons) is required to accurately capture leakage due to BTBT.[7] The implementation of the NEGF simulator is described in the Methods section. Figure 2c shows reasonable agreement within 1 order of magnitude between the experimental (solid circles) and the NEGF-simulated I_{MIN} (hollow circles) across 5 orders of magnitude of leakage. It should be noted that large-E_G CNTs > 0.9 eV are projected to have I_{MIN} < 0.1 pA/CNT, below the experimental noise floor.

The I_{MIN} also shows an exponential dependence on V_{DS} in Figure 2d,e. In the V_{DS} range of interest from −0.5 to −0.7 V, I_{MIN} changes by ∼1 order of magnitude. At moderate E_G = 0.64 eV, we observe I_{MIN} < 0.4 nA/CNT up to 0.7 V, which meets the high-performance I_{OFF} density target of 100 nA/μm for 250 CNTs/μm. However, there is no margin to further reduce the leakage current with V_{TH}. Figure 2e shows reasonable agreement between the experimental (solid circles) and the NEGF-simulated I_{MIN} (hollow circles) values in the V_{DS} range of interest for three different CNT band gaps. In the absence of BTBT, raising V_{DD} increases I_{OFF} by $10^{DIBL\times\Delta V_{DS}/S.S.}$, where DIBL is the drain-induced barrier lowering and SS is the subthreshold swing. For example, a Si FinFET with a DIBL of 45 mV/V and an S.S. of 69 mV/dec incurs only a ∼1.3× increase in I_{OFF} as V_{DD} increases from 0.5 to 0.7 V.[25] Similarly, in a CNT MOSFET without BTBT with a DIBL of 20 mV/V and an S.S. of 65 mV/dec, the I_{OFF} should increase by 1.2×.[17] However, if I_{OFF} at −0.5 V V_{DS} is initially equal to I_{MIN}, I_{OFF} will increase >10× at −0.7 V V_{DS} due to BTBT, which hinders energy-efficient device operation.

The dependence of the I_{MIN} on extension doping (n_{EXT}) is shown in Figure 2f,g. As V_{EXT} changes from negative to positive values, the extension changed from highly p-doped to lightly n-doped and MOSFET behaviors shift from p-type to highly resistive (Figure S4b). The nonmonotonic behavior of the I_{MIN} is caused by the change in the doping polarity and the leakage mechanism. For high to moderate n_{EXT} (labeled as region I in Figure 2f), I_{MIN} decreases with lower V_{EXT}. Figure 2g shows the reasonable agreement between the experimental (solid circles) and NEGF-simulated (hollow circles) I_{MIN} vs V_{EXT} for E_G = 0.58 and 0.74 eV in region I with medium to high n_{EXT}.

b. CNT Band Gap Is the Primary Tuning Knob in Controlling I_{MIN}. Compared with decreasing V_{DS} or n_{EXT}, increasing CNT band gap (E_G) is the most effective approach to reduce BTBT leakage, as a 0.25 eV increase in band gap reduces I_{MIN} by 1000× at −0.5 V V_{DS}, as shown in Figure 2c. On the other hand, V_{DS} can only change I_{MIN} by <100× in the V_{DD} range of interest (Figure 2d). While n_{EXT} can reduce I_{MIN} by more than 100× in the measurement window (Figure 2f), the tunable range of n_{EXT} is practically limited as reducing n_{EXT}

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also degrades the on-current (i.e., increasing the extension resistance). Considering a tight-binding approximation, the CNT band gap is inversely proportional to the CNT diameter by $E_G = \frac{0.85[\text{eV}\cdot\text{nm}]}{d_{CNT}[\text{nm}]}$.[43] As the CNT diameter is determined by (n,m) chirality, chirality sorting is a promising path to achieve leakage control through E_G selection.[44]

c. V_{DS} Effects Are Orthogonal to E_G and Dependent on Device Structure. Figure 2d shows that the I_{MIN} vs V_{DS} relation is similar for all CNT E_G from 0.35 to 1.19 eV, indicating that the two leakage modulation parameters are orthogonal. The orthogonality is also observed in a different device structure (Figure 3a), where the extension gate is placed on the same side of the top-gate electrode (i.e., top extension gate structure). 10 single-CNT MOSFETs with CNT E_G ranging from 0.43 to 0.96 eV and a top extension gate exhibit similar slopes of $\log(I_{MIN})$ vs V_{DS} regardless of E_G in Figure 3b. Figure S5 further confirms that the change in I_{MIN} due to V_{DS} is independent of E_G as the slope of $\log(I_{MIN})$ vs V_{DS} linear regression lines has no correlation with E_G for two different device structures.

However, the relation between V_{DS} and I_{MIN} depends on the device structure. The average slope of $\log(I_{MIN})$ vs V_{DS} in the top extension gate structure is smaller than that of the bottom extension gate structure, resulting in a smaller ΔI_{MIN} for a given ΔV_{DS} (Figure S5). This effect can be captured by a parameter called "tunneling distance" (i.e., distance between the conduction band in the channel and the valence band in the drain, measured at $E = E_{F\text{-}D}$ at 0 V V_{DS}). TCAD-simulated band diagrams in Figure 3c show that the top extension gate device structure has a longer tunneling distance than the bottom extension gate structure for the same E_G, thereby suppressing the increase in the BTBT leakage given the same ΔV_{DS}. The tunneling distance effects were investigated in four other device structures, as summarized in Figures S6 and S7 and Table S2. In the V_{DD} range of interest of 0.5−0.7 V, the tunable range of I_{MIN} increases from 2× to 30× as the tunneling distance decreases from 55 to 9 nm (Figure 3d). Hence, the tunneling distance is clearly the amplification factor of the V_{DS} effects on BTBT leakage. It is critical to consider the tunneling distance when engineering for low leakage.

d. n_{EXT} Determines the Dominant Leakage Mechanism. As n_{EXT} changes with V_{EXT} from high to low doping, the dominant leakage mechanism changes from BTBT to ambipolar tunneling. Figure 4 shows the NEGF-simulated band diagrams and the corresponding energy-resolved current spectra for source and drain contact positions at I_{MIN} for a 0.68 eV band gap and −0.5 V V_{DS}. The arrow in Figure 4a highlights the conduction path for phonon-assisted BTBT where the injected carriers at the source tunnel inelastically to the states in the channel, through the emission of one or multiple high-energy optical phonons (see Methods for the types of phonon included),[39,45] before tunneling to the drain extension at a high n_{EXT}. The conduction path is reflected in the current spectrum in Figure 4b where the drain current peaks around the Fermi level of the drain extension ($E_{F\text{-}D}$) at 0.5 eV, and the source current spectrum shows a peak at the source extension Fermi level ($E_{F\text{-}S}$) = 0 eV. At low n_{EXT}, the extension is nearly intrinsic, and no conduction is allowed between the CNT band gap (Figure 4c). Instead, electrons are injected at the drain contact, giving rise to ambipolar tunneling, which ultimately puts a lower bound on the minimum leakage, as shown by the peaks in Figure 4d.

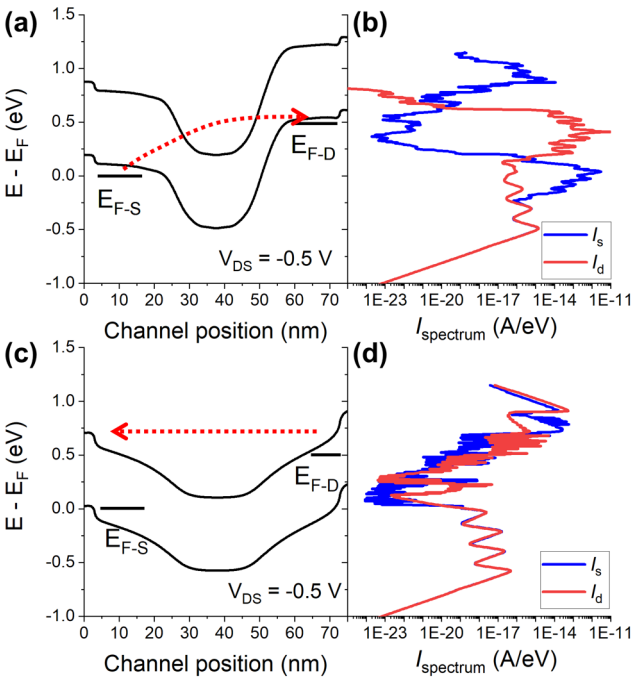

Figure 4. NEGF-simulated band profiles and energy-resolved current spectrum at I_{MIN} when V_{EXT} = −1.5 V (a,b) and V_{EXT} = 1 V (c,d) for E_G = 0.68 eV and V_{DS} = −0.5 V. The Fermi levels in the drain extension and source extension are labeled as $E_{F\text{-}S}$ and $E_{F\text{-}D}$. The dominant tunneling mechanism in (a) with high extension doping concentration is band-to-band tunneling (BTBT), while (c) shows ambipolar tunneling at a low extension doping level. The red arrows in (a,c) highlight the carrier conduction paths. At high extension doping, carriers injected at the source inelastically tunnel to the bound states in the channel before tunneling into the drain. At low extension doping, carriers are injected into the contacts, resulting in ambipolar tunneling. The multiple peaks present in both spectra at low energy are due to multiple optical phonon absorption/emission. To improve convergence, semi-infinite doped contacts are assumed as source and drain self-energies.[39] Degenerate doping is assumed in the first CNT rings to ensure proper boundary conditions even in the case of non-degenerate extension doping (e.g., Figure 4c).

e. Extension Doping Is Only Effective in Device Structures with Small Tunneling Distance. It should be noted that the above extension doping effects on BTBT leakage (Figure 2f,g) are only visible for small tunneling distances (<10 nm). For example, in the device structure with a top extension gate and 24 nm tunneling distance, as shown in Figure 3a, there was no observed I_{MIN} dependence on V_{EXT} as the change in BTBT leakage is suppressed by the long tunneling distance for both high and low n_{EXT} (Figure S8).

IV. CNT MOSFET NEGF Leakage Current Projection. To project the overall on- and off-current trends as a function of E_G, n_{EXT}, and V_{DS}, we experimentally calibrated an NEGF model for a top-gated CNT MOSFET with chemically doped, step-like extensions. While the experimental portion of this study uses electrostatic doping to induce tunable doping levels in the extension region, integrated CNT MOSFETs need to rely on solid-state doping to avoid additional parasitic capacitance.[13,38] We therefore first model the impact of a uniform step-like n_{EXT}, analogous to what could be obtained by solid-state doping. The chemical extension doping effects depend on V_{DS} and the CNT band gap and are similar to

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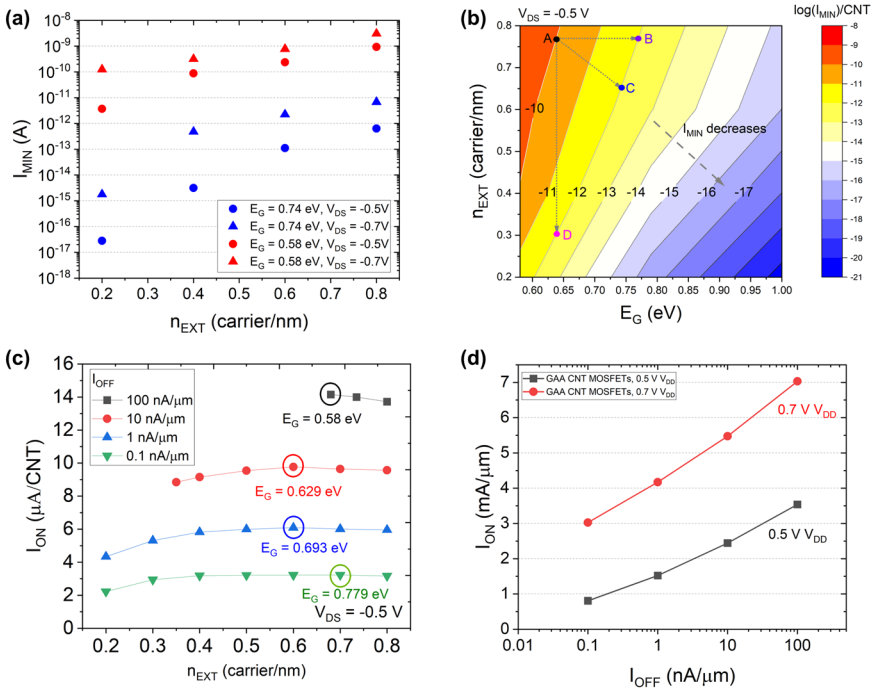

Figure 5. (a) NEGF-simulated I_{MIN} at 300 K versus n_{EXT} for E_G = 0.58 and 0.74 eV based on the calibrated NEGF model for the same device structure in Figure 2a without the bottom extension gate. (b) NEGF projection of I_{MIN} versus n_{EXT} and E_G for long-channel top-gate CNT MOSFETs with short tunneling distance at V_{DS} = −0.5 V based on the NEGF model calibrated to this work's leakage data. Point A is one example design choice to achieve I_{MIN} = 0.1 nA/CNT. Points B−D are three alternative design choices to lower the I_{MIN} to 1 pA/CNT. (c) Projection of I_{ON} at a given I_{OFF} density based on compact modeling (Table 1) at V_{DS} = −0.5 V. I_{ON} is simulated based on the sampled (n_{EXT}, E_G) combinations along the same I_{MIN} contour line and plotted against n_{EXT} at −0.5 V V_{DS}. Doping-dependent contact resistances were assumed based on NEGF simulations[46] calibrated to experimental data.[12] All points on a given line in (c) correspond to the same I_{OFF} density. The circled data points represent the (n_{EXT}, E_G) combinations with the highest I_{ON} at the specified I_{OFF} density. (d) Projection of I_{ON} based on the compact model (Table 1) versus NEGF-projected I_{OFF} for gate-all-around (GAA) CNT MOSFETs. The curves represent accessible on/off-current density on the I_D−V_{GS} curve by V_{TH} shift with a window size of V_{GS} = V_{DS} = V_{DD} for GAA CNT MOSFETs at 0.5 V (black) and 0.7 V (red) V_{DD}.

electrostatic doping experimental data. In the n_{EXT} range of interest from 0.2 to 0.8 carrier/nm, the tunable range of NEGF-simulated I_{MIN} increases from 30× to 300× as V_{DS} decreases from −0.5 to −0.7 V for a 0.58 eV band gap (Figure 5a). The ΔI_{MIN} from n_{EXT} is more significant for larger band gap CNT, reaching 3−4 orders of magnitude for E_G = 0.74 eV.

Next, the BTBT leakage current of CNT MOSFETs with small tunneling distance is projected based on the NEGF model validated with I_{MIN} data in the previous sections. We focus on the small tunneling distance as it corresponds to the highest possible level of leakage and represents the most pessimistic projection for leakage current. Figures 5b and S9 show the NEGF-simulated I_{MIN} contour map for E_G from 0.58 to 1.0 eV and n_{EXT} from 0.2 to 0.8 carriers/nm at −0.5 and −0.7 V V_{DS} respectively. The design space projection maps the sensitivity of I_{MIN} with respect to each tuning knob.

As the isocurrent lines are denser at the bottom right corner of the contour plot, ΔI_{MIN} is larger at lower n_{EXT} and larger band gap. E_G is more effective in controlling I_{MIN} than n_{EXT} as the horizontal isocurrent line spacing is much smaller than the vertical spacing. Based on the performance requirements and the leakage specifications, device and circuit designers can choose the appropriate combination of E_G, n_{EXT}, and V_{DD}. For example, at −0.5 V V_{DS} and 0.77 carriers/nm, increasing the band gap from 0.64 to 0.76 eV reduces the I_{MIN} from 100 to 1 pA/CNT (point A to B in Figure 5b). The same reduction in I_{MIN} can also be achieved by lowering n_{EXT} from 0.77 to 0.3 carriers/nm while keeping E_G constant (point A to D) or increasing E_G to 0.74 eV and decreasing n_{EXT} to 0.65 carriers/nm at the same time (points A to C). Device engineers may select the appropriate design choices based on the target application, the material availability, and on-current requirements. This design space projection of leakage current is specific to CNT MOSFETs with long-channel (gate length >20 nm) where source-drain tunneling is negligible and tunneling distance is small (<10 nm). Devices with longer tunneling distances are less sensitive to n_{EXT}. Device structures can be engineered to increase the tunneling distance for BTBT leakage suppression with associated trade-offs in other device characteristics such as on-state current, device footprint, and parasitic resistance.

To understand the trade-offs between transport and leakage and evaluate different design choices, a compact model[41,42] is utilized to project on-current and identify the design choices for optimizing on-current at a constant off-current density. The model input parameters are summarized in Table 1. Doping-dependent contact resistance of 3.55−5.86 kΩ/CNT was assumed for n_{EXT} from 0.8 to 0.2 carriers/nm based on NEGF simulations[46] calibrated to experimental data[12] (Figure S10). The impact of doping is also included in the model for the extension resistance.[46] For I_{on} projection, we consider a gate-all-around (GAA) geometry (Figure S11), which is projected to achieve larger energy-delay benefits than top-gate geometry.[7] Given a degenerate extension doping level, the

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Table 1. Compact Modeling Parameters for the I_{ON} Projection

Parameters	Assumptions
CNT density	250 CNTs/μm
L_C	100 nm
L_G	20 nm
L_{EXT}	25 nm
R_C	Doping-dependent, experimentally calibrated TCAD[46] 3.55−5.86 kΩ/CNT
R_{EXT}	Virtual-source CNFET model[41,42]
Gate dielectric	2.5 nm HfO_2 + 0.5 Al_2O_3
C_{OX}	2.94×10^{-10} F/m

GAA geometry has a minimal impact on the relations among I_{MIN}, E_G, V_{DS}, and n_{EXT} compared to a top-gate geometry. Different combinations of (n_{EXT}, E_G) are selected as the simulation inputs by traversing along the I_{MIN} contour lines (Figure S12a). The V_{TH} is shifted to set $I_{OFF} = I_{MIN}$ at $V_{GS} = 0$, and I_{ON} is extracted at $V_{GS} = V_{DS} = V_{DD}$. I_{ON} values for the selected (n_{EXT}, E_G) combinations are shown in Figures 5c and S12b at four I_{OFF} densities. The (n_{EXT}, E_G) design choices with the highest I_{ON} at a given I_{OFF}, as circled in Figures 5c and S12b, are also marked on the I_{MIN} contour map in Figure S12c,d. The results indicate that to enhance the on-current, $n_{EXT} > 0.5$ nm^{-1} is required at a given I_{OFF}. Figure 5d highlights the accessible on-current and off-current density in GAA CNT MOSFETs for I_{OFF} limited by BTBT between 0.1 and 100 nA/μm at 0.5 and 0.7 V V_{DD}, achieving highest $I_{ON} = 7.03$ mA/μm at 0.7 V V_{DD}.

CONCLUSION

In summary, the BTBT leakage current I_{MIN} in CNT MOSFETs was measured and analyzed as a function of the CNT band gap, supply voltage, extension doping, and device architecture. A calibrated NEGF model captures the BTBT leakage's dependence on these factors and projects the design space of leakage current. The design space projection identifies the design choices for high-performance and low-energy applications and the strategies to reduce leakage. CNT band gap is found to be more effective in controlling I_{MIN} than supply voltage. The extension doping effects are significant only for MOSFET device structures with short tunneling distances, and the tunneling distance can be further optimized to lower BTBT leakage. Adding on-current projection to the leakage current design space identifies the best design choices for optimizing on-current at a given off-current density. Future work should investigate source-drain tunneling contribution to extend the leakage analysis to short-channel CNT MOSFETs with a sub-20 nm gate length.

METHODS

Fabrication of top-gate CNT MOSFETs with a bottom extension gate consists of two parts: (1) optical lithography to define contact pads on 100 mm wafers, which were later diced into chips; (2) electron-beam lithography to define source/drain contacts, active region, and top-gate electrodes.

Fabrication of Small Chips with Gate and Contact Pads. 13 nm silicon oxide was grown on a 100 mm Si wafer using dry thermal oxidation. Optical lithography was used to pattern the bottom extension gate pads, source/drain contact pads, and wires. Electron-beam evaporation and liftoff were used to deposit 1 nm Ti and 30 nm Pt. A 4.7 nm Al_2O_3 bottom-gate dielectric was deposited via atomic layer deposition (ALD) at 200 °C. Vias were patterned through the Al_2O_3 dielectric using optical lithography followed by plasma etching in $CF_4/CHF_3/Ar$ to probe the gate and contact pads. The Si wafer was then diced in to 1.4 × 1.4 cm chips for electron-beam lithography.

CNT Growth and Transfer. Aligned carbon nanotubes were grown by a CVD process at 900 °C on ST-quartz substrate using an ethanol carbon source and iron catalyst with sample preparation similar to Patil et al.[37] The CNTs were transferred onto the small chips using thermal release tapes and 100 nm Au as the sacrificial layer.[37] Scanning electron microcopy (SEM) and atomic force microscopy (AFM) were used to determine the average CNT line density, which was around 2−3 CNTs/μm.

Define Source/Drain Contacts, Active Region, and Top Gate. Electron-beam lithography was used to define 200 nm long source/drain contacts; 30 nm Pd film was deposited to form p-type contacts using electron-beam evaporation. The active region was defined by patterning a bilayer resist consisting of poly(methyl methacrylate) (PMMA A2) and MaN 2405 (diluted 1:1 in anisole). The MaN was patterned using electron-beam lithography into a stripe between 300−500 nm wide, depending on the average CNT line density, and developed in 2% TMAH. CNTs not covered by the MaN stripe were etched away by O_2 plasma, achieving a single-CNT channel. 1.3 nm nanofog Al_2O_3[17] and 2.5 nm HfO_2 were deposited via atomic layer deposition (ALD) as a top-gate dielectric. Vias were patterned through the Al_2O_3/HfO_2 dielectric using optical lithography followed by wet etching in 6:1 buffered-oxide-etchant (BOE) to probe the contact pads. Electron-beam lithography was used to define the 100 nm long top-gate. 30 nm Pd film was deposited by electron-beam evaporation as top-gate electrodes.

Measurements of CNT MOSFETs. Top-gate CNT MOSFETs were measured in compressed dry-air using a Cascade semiauto probe station and a Keysight B1500A semiconductor parameter analyzer to screen the working devices. The yielded devices were then measured in vacuum using a Lakeshore cryoprobe station and a Keysight B1500A semiconductor parameter analyzer from 10 K to room temperature.

NEGF Simulations. The simulations are carried out by self-consistently solving the Poisson equation and the Schrödinger equation through the NEGF formalism in a three-dimensional (3D) space. The 3D potential profile is derived by solving the Poisson equation considering the free carriers and dopant charges. The Hamiltonian H employed is based on tight-binding approximation in the mode space (leveraging the cylindrical geometry of the CNT p_z orbitals),[45] with a nearest-neighbor hopping parameter $t = 3$ eV and considering the first two sub-bands (one for each spin). Within the NEGF formalism, the retarded Green's function G is derived as

$$G(E) = [EI - H - \Sigma(E)]^{-1}$$

where E is the energy, I is the identity matrix, and $\sum$ is the summation over the self-energies for each relaxation mechanism (including source/drain contacts, acoustic phonon scattering, and optical phonon scattering):

$$\Sigma(E) = \Sigma_S(E) + \Sigma_D(E) + \Sigma_{scat}(E)$$

The derivation of $\sum_{scat}$ is detailed in ref 39. The phonon scattering mechanisms considered are described in Table 2.

Table 2. NEGF Simulation Parameters

Mechanism	Energy	Intraband or Interband	Coupling
LO	190 meV	Intra	$0.0172-4.66 \cdot 10^{-4} \cdot$ chirality
RBM	28 meV/diameter	Intra	$0.0013-0.48 \cdot 10^{-4} \cdot$ chirality
LO/TA	180 meV	Inter	$0.0329-8.62 \cdot 10^{-4} \cdot$ chirality
LA	Acoustic	Intra	$0.0041-1.08 \cdot 10^{-4} \cdot$ chirality

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The coupling coefficient has been extrapolated following the results presented in ref 39.

The simulations are executed with two nested loops: the external loop solves self-consistently the Poisson equation and the Schrödinger equation within the NEGF formalism; the internal loop solves self-consistently the NEGF equation considering phonon scattering. At first, the simulations are carried out in the ballistic regime until a self-consistent solution of the potential is found. The potential and the ballistic energy- and position-dependent electron−hole distributions are used as inputs to derive the self-energies of scattering. The NEGF equations are solved until the charge in the system converges without modifying the potential. Once a self-consistent solution of the electron/hole distributions is found, the Poisson equation is solved, and the new potential is used as input to a new iteration of the dissipative NEGF, until a final self-consistent potential is found.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.3c04346.

Dominant leakage mechanisms in CNT MOSFETs, previous literature that studys CNT transistor leakage behaviors, process flow for top-gate CNT MOSFETs, the CNT band gap extraction method, electrical characterizations of CNT MOSFETs at different supply voltages, the linear regression slope of $\log(I_{MIN})$ versus V_{DS}, cross-section schematics of CNT MOSFETs with different extension gate configurations, summary of the six device structures of CNT MOSFETs, I_{MIN} versus V_{DS} for six different device structures, I_{MIN} vs V_{EXT} for a single-CNT top-gate MOSFET with a top extension gate, NEGF projection of I_{MIN} for long-channel top-gate CNT MOSFETs with short tunneling distance at V_{DS} = −0.7 V, contact resistance at different extension doping levels based on NEGF simulations, 3D view and cross-section view of the gate-all-around (GAA) MOSFETs, projection of on-current for GAA CNT MOSFETs at given off-current densities (PDF)

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Author Contributions

Q.L., C.G., G.P., and H.-S.P.W. conceived and planned the project with inputs from I.R. and S.M. Q.L. fabricated the devices, performed the electrical characterization and data analysis, and wrote the manuscript. C.G. performed the NEGF and compact model simulation. S-k.S. performed the TCAD simulation with support from E.C. The gate oxide processing was supported by Z.Z., P.B., and A.K. All authors have given approval to the final version of the manuscript. Q.L. and C.G. contributed equally.

Notes

The authors declare no competing financial interest.

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