Border trap analysis and reduction in ALD-high-k InGaAs gate stacks

Kechao Tang[1], Adi Negara[1], Tyler Kent[2], Ravi Droopad[3], Andrew C. Kummel[2], and Paul C. McIntyre[1]

[1]Department of Materials Science and Engineering, Stanford University, Stanford, CA 94305
[2]Department of Chemistry and Biochemistry, University of California, San Diego, La Jolla, CA 92093
[3] Ingram School of Engineering, Texas State University, San Marcos, TX 78666
E-mail address of corresponding author: pcm1@stanford.edu

For future high performance III-V n-channel MOS devices, $In_{0.53}Ga_{0.47}As$ is a promising material for the channel due to its high electron mobility and moderate band gap. Atomic layer deposited (ALD) Al_2O_3 has a large conduction band offset to InGaAs and can form a low defect-density interface with InGaAs [1]. ALD-HfO_2 can achieve a very low EOT and low gate leakage [2]. Therefore, both of these oxides have received extensive attention as candidate dielectric layers for InGaAs nMOSFETs. Apart from the well-known effects of oxide/InGaAs interface charge traps that may pin the Fermi level of the channel, traps in the oxide layer, often called border traps, may also reduce the charge in the channel and thus degrade the on-state performance of InGaAs MOSFET devices. In this presentation, we study the effects of various approaches to reduce the border traps, like variation of ALD temperature, post-gate metal forming gas (5% H_2/95% N_2) anneals (FGA), and bias-temperature electrical stress.

Experimental methods employed include quantitative interface trap and oxide trap modeling [3, 4] of MOS capacitor data obtained over a range of frequencies and temperatures. With the application of these models, we find that the border trap density (N_{bt}) in ALD Al_2O_3 depends strongly on ALD temperature. Fig. 1 shows the multi-frequency CV curves for post-metal FGA treated Pd/Al_2O_3/InGaAs samples in which the gate dielectric was deposited at different ALD temperatures. MOS capacitors fabricated using trimethylaluminum (TMA)/H_2O at an ALD temperature of 120°C have a considerably lower N_{bt} while maintaining a similarly low interface trap density (D_{it}) compared to samples prepared with a more standard 270°C Al_2O_3 ALD temperature. Large-dose TMA exposure (pre-dosing) prior to Al_2O_3 ALD is also found to be an important step to guarantee stable electrical quality of the low temperature-deposited samples.

Considering other possible defect passivation approaches, we carry out a systematic study of the effects of post-gate forming gas anneal (FGA) time and temperature on the density of interface and border traps in Al_2O_3/InGaAs gate stacks. It is found that FGA at 400°C for 30 min saturates the effect of FGA on Al_2O_3/InGaAs. Fig. 2 shows that increasing the FGA time slightly reduces the D_{it}, but has little effect on the N_{bt}. In addition, preliminary results on the effects of bias-temperature stress on Al_2O_3/InGaAs will be reported.

For the ALD-HfO_2 MOS structures, we examine the dependence of D_{it} and N_{bt} on 1) the InGaAs surface orientation, 2) HfO_2 ALD temperature, and different substrate surface treatment procedures. Fig. 3 demonstrate that for ALD HfO_2 on both InGaAs (001) surface and (110) surface, the D_{it} response decreases dramatically when the measurement temperature is lowered from room temperature to -40°C, while the N_{bt} shows little variations. This result indicates that interface traps and border traps are two different types of defects, which is also supported by another experiment in which we found that increasing the cycle number of in-situ plasma H/TMA/H [5] cleaning cycles prior to HfO_2 ALD significantly reduces the D_{it} but has little impact on N_{bt}. In addition, we systematically compared the N_{bt} of HfO_2 to that of ALD Al_2O_3. Fig. 4 displays the energy distribution of N_{bt} in the HfO_2 and Al_2O_3 layers investigated in this study. Comparing each of the dielectrics we have studied, HfO_2 has an N_{bt} value that is ~3 times larger than that of Al_2O_3.

In conclusion, we have found that Al_2O_3 deposited on InGaAs with lower ALD temperature has significantly reduced N_{bt}, and the N_{bt} of HfO_2 is around 3 times larger than that of Al_2O_3. The N_{bt} of HfO_2 is independent of measurement temperature, similar to our previous result on Al_2O_3/InGaAs gate stacks. Our current work focuses on understanding the physical mechanism under the ALD temperature effect on the N_{bt} of Al_2O_3.

References

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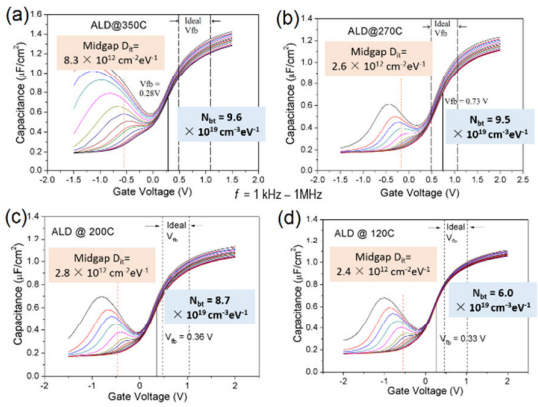

Fig. 1: Multi-frequency (1 kHz – 1 MHz) CV curves for $Pd/Al_2O_3/InGaAs$ samples with Al_2O_3 ALD temperature at (a) 350℃, (b) 270℃, (c) 200℃ and (d) 120℃ respectively. D_{it} is extracted [3] at energy level of $E - E_c$ = -0.45 eV, and N_{bt} is extracted [4] at energy level of $E - E_c$ = 0.50 eV.

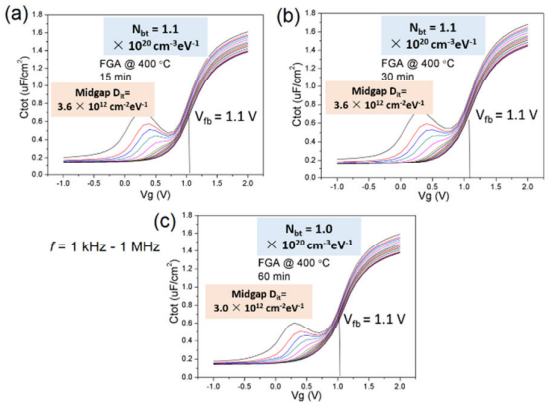

Fig. 2: Multi-frequency (1 kHz – 1 MHz) CV curves for $Pd/Al_2O_3/InGaAs$ gate stacks with different FGA time. N_{bt} is extracted at energy level of $E - E_c$ = 0.50 eV.

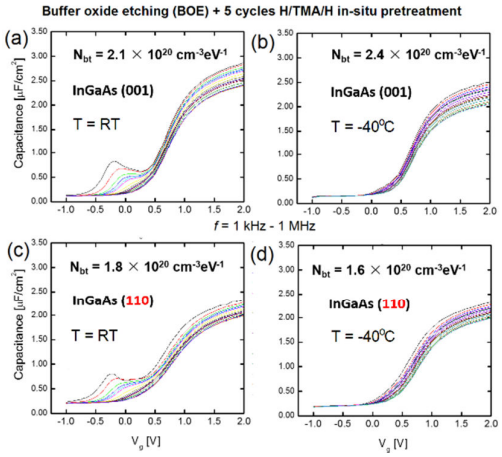

Fig. 3 : Multi-frequency (1 kHz – 1 MHz) CV curves for $HfO_2/InGaAs$ MOS capacitors with InGaAs(001) (a - b) and InGaAs(110) (c - d) orientations at room temperature and -40°C. N_{bt} is extracted at energy level of $E - E_c$ = 0.50 eV.

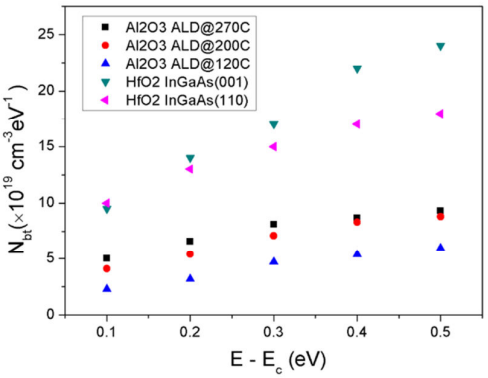

Fig. 4: Energy distribution of N_{bt} for Al_2O_3 on InGaAs with various ALD temperatures and HfO_2 deposited on InGaAs of different surface orientations.