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In Situ Observation of Initial Stage in Dielectric Growth and Deposition of Ultrahigh Nucleation Density Dielectric on Two-Dimensional Surfaces

Jun Hong Park,[†] Hema C. P. Movva,[∥] Evgeniy Chagarov,[‡] Kasra Sardashti,[†] Harry Chou,[∥] Iljo Kwak,[†] Kai-Ting Hu,[§] Susan K. Fullerton-Shirey,[⊥] Pabitra Choudhury,[#] Sanjay K. Banerjee,[∥] and Andrew C. Kummel*[,†,‡]

[†]Materials Science & Engineering Program, [‡]Departments of Chemistry & Biochemistry, and [§]Mechanical and Aerospace Engineering, University of California, San Diego, California 92093, United States

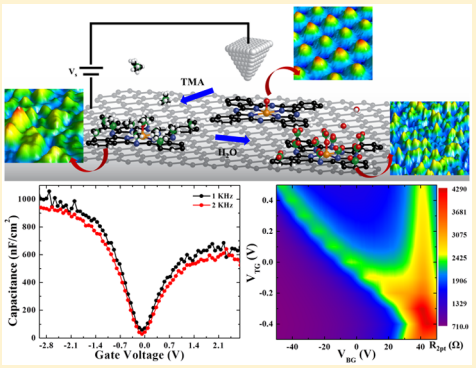
[∥]Electrical and Computer Engineering, University of Texas at Austin, Austin, Texas 78712, United States

[⊥]Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556, United States

[#]Department of Chemical Engineering, New Mexico Tech, Socorro, New Mexico 87801, United States

Supporting Information

ABSTRACT: Several proposed beyond-CMOS devices based on two-dimensional (2D) heterostructures require the deposition of thin dielectrics between 2D layers. However, the direct deposition of dielectrics on 2D materials is challenging due to their inert surface chemistry. To deposit high-quality, thin dielectrics on 2D materials, a flat lying titanyl phthalocyanine (TiOPc) monolayer, deposited via the molecular beam epitaxy, was employed to create a seed layer for atomic layer deposition (ALD) on 2D materials, and the initial stage of growth was probed using *in situ* STM. ALD pulses of trimethyl aluminum (TMA) and H_2O resulted in the uniform deposition of AlO_x on the TiOPc/HOPG. The uniformity of the dielectric is consistent with DFT calculations showing multiple reaction sites are available on the TiOPc molecule for reaction with TMA. Capacitors prepared with 50 cycles of AlO_x on TiOPc/graphene display a capacitance greater than 1000 nF/cm^2, and dual-gated devices have current densities of 10^{-7}A/cm^2 with 40 cycles.



KEYWORDS: *Dielectric, graphene, TiOPc, STM, ALD, capacitance*

Complementary metal−oxide−semiconductor (CMOS) technology based on Si has been implemented for logic devices due to its outstanding performance and low cost. However, as CMOS devices are scaled down to a few nanometers, the maximum density of devices is limited by the power consumption of each device. To develop alternative, low-voltage devices with steeper subthreshold swing than the 300 K thermodynamic limit of 60 mV/decade, devices with graphene as the channel material are being explored.[1,2] Graphene has high carrier mobility and stability; therefore, most research has been focused on graphene devices based on in-plane transport.[1−4] However, due to the zero band gap of graphene, such devices cannot be turned OFF and are hence not directly useful for CMOS architectures.

An alternative approach uses vertical junctions in a 2D/insulator/2D geometry, relying on charge transfer out of the plane and offering potential for low OFF-state power consumption. Device structures such as the bilayer pseudospin field-effect transistor (BiSFET) and the interlayer tunneling FET based on 2D materials have been proposed.[5−16] 16 Although the layout of each device is different, all device models share a common vertical 2D/I/2D structure. In order to fabricate these vertical junctions, a high quality ultrathin (1−2 nm) insulating layer must be inserted between two 2D layers.[6−10,12−14,17−19] Although graphene/insulator/graphene junctions with mechanically exfoliated hexagonal boron nitride have shown negative differential resistance (NDR) when appropriately biased,[11,18,20] there are still few reports of NDR due to the poor reproducibility.[8,9,12,18] Moreover, the mechanical transfer of exfoliated layers and subsequent assembly of stacks requiring rotational alignment are unrealistic for large-scale device production.[18] To overcome these challenges, atomic layer deposition (ALD) has been proposed to deposit a dielectric.[12,13,19,21,22] However, most of the previous research on ALD dielectrics on 2D materials has focused on thick layers (>10 nm) because most 2D materials do not have dangling bonds, and thin dielectrics give rise to large pinhole densities.[23−29] Although the initial growth stage is

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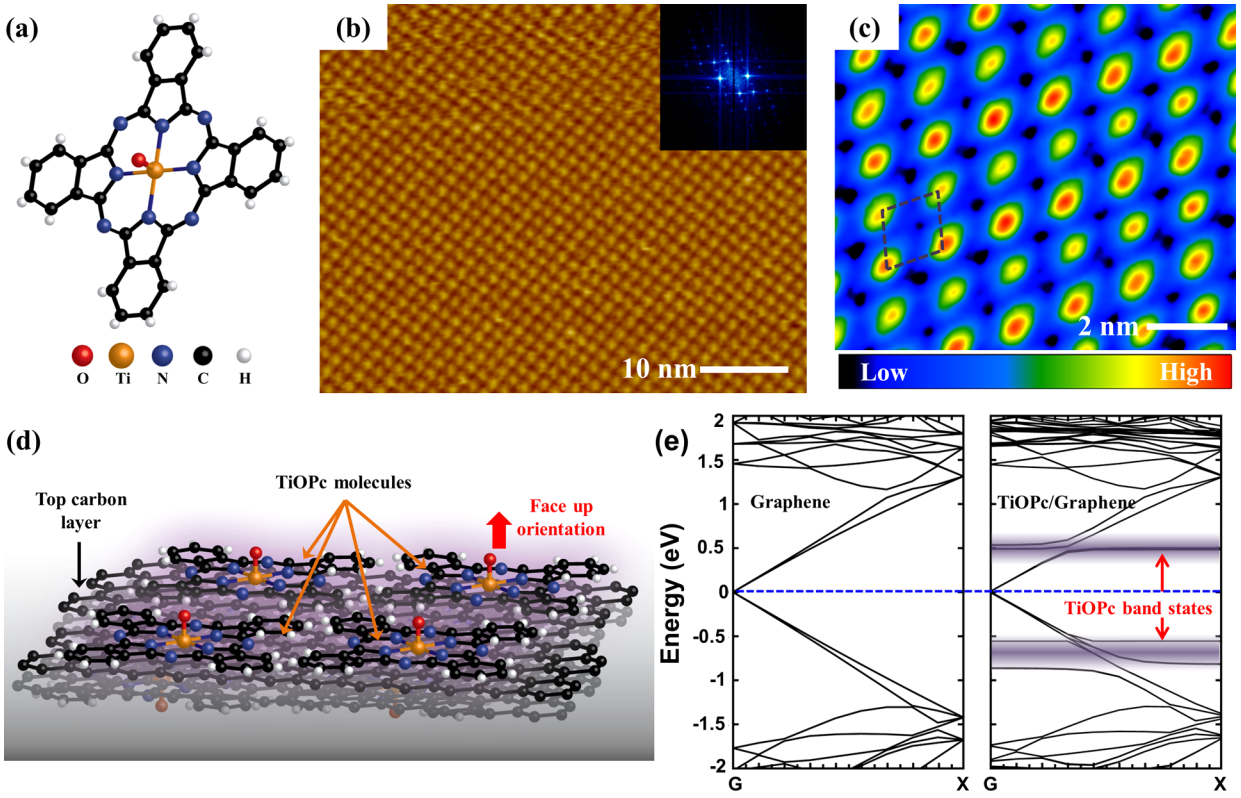

Figure 1. Empty state STM images of monolayer TiOPc on HOPG and band structure of graphene and TiOPc/graphene. STM images recorded with V_S = +2.0 V, I_T = 20 pA at 100 K. (a) Schematic model for the molecular structure of TiOPc. (b) Bare TiOPc monolayer deposited by MBE on HOPG. The inset shows the Fourier transform (FT) of the TiOPc monolayer. (c) Submolecular resolution of MBE TiOPc monolayer. The central bright spot is assigned to O. (d) Schematic sketch of TiOPc monolayer, including the HOPG. (e) DFT band structure of graphene before (left) and after (right) deposition of TiOP on graphene. The position of E_F is shown with the blue dashed line.

critical to deposit pinhole-free, thin dielectrics, the direct observation of ALD nucleation on 2D materials has not yet been reported at the atomic level because ALD precursors are readily transformed into an oxide in ambient air and easily transfer from 2D materials to STM tips even at low temperatures.

To nucleate ultrathin dielectrics uniformly on 2D materials, titanyl phthalocyanine (TiOPc) molecules are deposited on graphite and graphene as a template for ALD dielectrics. Each step of the deposition of both TiOPc and the dielectric are observed at the molecular scale with *in situ* STM in ultrahigh vacuum to overcome the extreme reactivity of the ALD precursor in ambient air. Using the TiOPc seed layer, graphene capacitors and FETs were fabricated to evaluate the electrical properties of the deposited dielectrics. Combing in situ observation, the growth of thin dielectrics on TiOPc/graphene can be extended to interlayer FETs based on transition metal dichalcogenides (TMD).[15,30−33]

Highly oriented pyrolytic graphite (HOPG) was purchased from SPI supplies (Structure Probe, Inc.). TiOPc was purchased from Sigma-Aldrich and purified by multiple sublimations. To obtain a clean surface, HOPG samples were exfoliated multiple times in air. Monolayer graphene films were grown by chemical vapor deposition (CVD) and transferred onto highly N-doped SiO_2/Si substrates. After loading into the UHV deposition chamber, both the HOPG and graphene samples were heated to 750 K for 3 h to remove volatile organic contaminants and other adsorbates. A thick overlayer of TiOPc was deposited on clean HOPG or graphene at 373 K using organic molecular beam epitaxy (MBE) with a differentially pumped effusion cell (Eberl MBE-Komponenten) as shown in Figure S1. Subsequently, the thick multilayer was heated to 523 K for 6 min, and a flat-lying TiOPc monolayer was formed. It is noted the TiOPc monolayer also can be obtained by solution dip coating, as shown in Figure S2, but more uniform, flat lying domains were obtained by UHV MBE deposition. ALD reactions on the TiOPc monolayer were performed with an *in situ* ALD system attached to the UHV system to avoid air exposure. The TiOPc/HOPG was transferred from the UHV chamber to the ALD chamber via a load-lock chamber, without breaking vacuum. After exposure to trimethyl aluminum (TMA) of various pulse durations (70 to 360 ms) and H_2O pulses of 500 ms duration at 373 K, the samples were transferred back to the STM stage, again without air exposure. STM and STS were performed at 100 K with an Omicron VT STM system with etched tungsten tips. Capacitors were fabricated using CVD-grown graphene, while dual-gated FETs were fabricated on exfoliated, monolayer graphene on Si/SiO_2 using e-beam lithography (50 nm Ni top gate contacts). Both the graphene capacitors and FETs were annealed at 623 K for 8 h in vacuum (~1 × 10^{-6} Torr) to remove resist residue remaining from device fabrication. The cleaned samples were transferred into the UHV chamber to deposit a TiOPc seed layer. Afterward, these samples were transferred in ambient air to a commercial ALD reactor (Beneq) to form the AlO_x/TiOPc/graphene/SiO_2/Si stack. After dielectric deposition, Ni was deposited on AlO_x/TiOPc graphene/SiO_2/Si as the top-gate using a thermal evaporator. All electrical measurements were performed with a probe station in ambient conditions.

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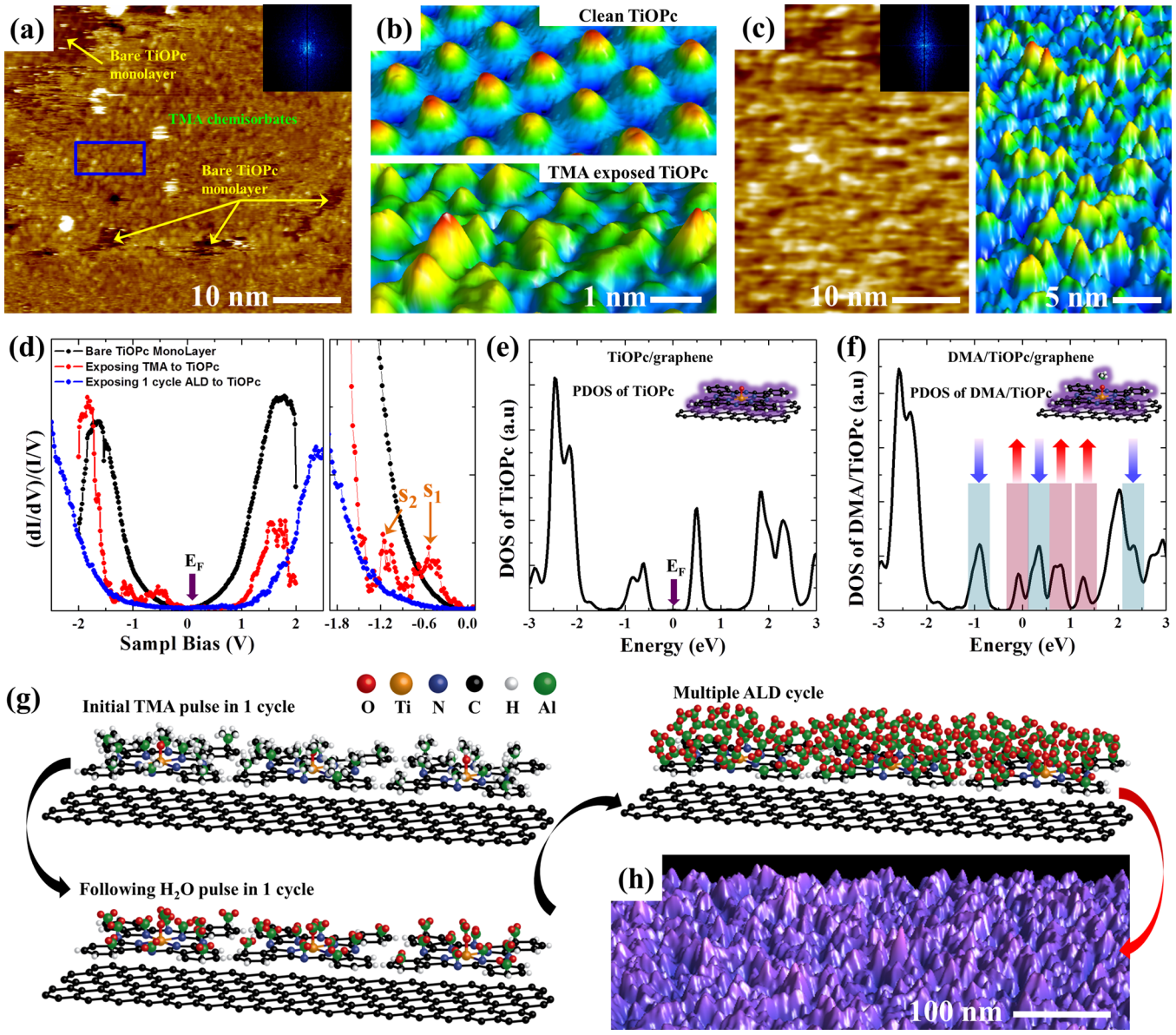

Figure 2. Topographic and electronic transitions for exposure of TMA and 1 cycle of ALD on TiOPc/HOPG. (a) TiOPc monolayer exposed to TMA for 70 mS at 373 K. STM images recorded with V_S = +2 V, I_T = 20 pA at 100 K. The inset shows the Fourier transform (FT) of the DMA/TiOPc. (b) Three-dimensional STM image with molecular resolution. Upper, bare TiOPc monolayer; lower, TMA exposed surface on TiOPc/HOPG from enlarged rectangular area from panel (a). (c) TiOPc/HOPG monolayer exposed to 1 cycle of ALD at 373 K with TMA for 360 ms and H_2O for 500 ms. STM images recorded with V_S = +3 V, I_T = 20 pA at 100 K. The inset shows the FT of the AlO_x/TiOPc. The right image shows a 3D expanded STM image of the one cycle of ALD on the TiOPc/HOPG. (d) STS dI/dV/I/V spectrum of bare, exposed TMA, and one cycle of ALD pulse (TMA + H_2O) on TiOPc monolayer. On the right, the close up view of STS from −2.1 to 0.1 V shows band gap states corresponded C_1 and C_2. (e,f) DFT projected density of states (PDOS) of a TiOPc molecule and a DMA/TiOPc molecule on graphene, respectively, assuming a single DMA molecule reacts only with the O of the TiOPc molecule. (g) Proposed schematic diagram for growth of AlO_x on TiOPc/graphene. (h) AFM images after five cycles of ALD pulse on TiOPc/single layer graphene/SiO_2/Si.

Density functional theory (DFT) calculations were carried out using the Vienna *ab initio* simulation package (VASP).

A highly ordered TiOPc monolayer is deposited on HOPG by UHV-MBE as confirmed by STM. A schematic diagram of the TiOPc molecular structure is shown in Figure 1a, and details explanation of structure are contained in Figure S3. Figure 1b shows an empty-state STM image with a defect-free monolayer of TiOPc deposited on HOPG with long-range order. Although most of the STM experiments in this study have been done on graphite, both graphite and graphene surfaces are inert due to sp^2 hybridization[29] and can therefore be considered equivalent for this study. The Fourier transform (FT) of Figure 1b is provided in the inset, where a distinct set of peaks is consistent with an array of single-phased crystalline TiOPc. Figure 1c shows that the TiOPc molecules form a square lattice; however, because of both thermal drift and piezo creep, the STM and FT images are distorted from a square to a rhombus. Each individual TiOPc molecule has a bright spot at its center, assigned to O, and darker surrounding features assigned to the aromatic rings, indicating that the TiOPc molecules face vacuum to form a flat-lying monolayer as shown in the schematic diagram of Figure 1d. In addition to graphite, TiOPc monolayers can also be obtained on TMD surfaces, as shown in Figure S7. As shown in previously reported DFT

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calculations, the outer benzene rings of TiOPc molecules provide weak $\pi-\pi^*$ interaction with the substrate, while the central O and N are negatively charged, thereby providing potential binding sites for polar adsorbates.[34]

DFT calculations show that TiOPc on graphene does not induce major electronic perturbation in the band structure of graphene close to the Dirac point. Figure 1e shows the band structures of both graphene (left) and TiOPc/graphene (right) with the position of the Fermi level marked by a blue dashed line. The details of the DFT calculations are include in the Supporting Information. After deposition of the TiOPc monolayer on graphene, new band states corresponding to TiOPc are generated; however, the symmetric linear dispersion of the graphene band structure, which is critical for a vertical junction, are nearly unchanged.[10] The band-decomposed charge density near the Dirac point of TiOPc/graphene is shown in Figure S8, providing further confirmation of unchanged band structure of graphene.

After verifying the deposition of an ordered seed layer of TiOPc, AlO_x dielectric was deposited using ALD. TMA exposure to TiOPc/HOPG for 70 ms at 373 K induces chemisorbate islands, as illustrated in the empty state STM image in Figure 2a consistent with the dissociation of TMA into dimethyl aluminum (DMA). Note, the dissociation of TMA can occur even at 300 K, indicating that there are dissociated chemisorbates on the TiOPc/HOPG after exposure to TMA at 373 K.[35,36] Figure 2b shows a three-dimensionally (3D) rendered, high-resolution STM image of the TiOPc/HOPG surface before and after exposure to TMA. Before TMA exposure, each TiOPc molecule has a uniform appearance in the STM image, with an average spacing of 1.6 ± 0.02 nm in a periodic array. However, after TMA exposure, there is no apparent periodicity, and the surface comprising an adsorbate/TiOPc complex has features of varying height and spacing. As shown in the inset of Figure 2a, the FT of the STM image shows diminished peak intensity compared to the FT of unreacted TiOPc/HOPG of Figure 1a. The chemisorbate/TiOPc complexes have an average spacing of 1.25 ± 0.05 nm, which is less than the spacing between bare TiOPc molecules on HOPG, consistent with multiple binding states for the ALD precursor on a single TiOPc molecule. The schematic diagram for the proposed process of forming amorphous TMA/TiOPc/HOPG surface is shown in Figure S12 in the Supporting Information.

Because the TiOPc monolayer is highly reactive to TMA, high-density AlO_x nucleation on TiOPc/HOPG results even after just one pulse of TMA and H_2O. Formation of stoichiometric Al_2O_3 requires a postannealing step, and therefore, the aluminum oxide formed on the surface is denoted as AlO_x.[37,38] As shown in STM and 3D rendered STM images of Figure 2c, after one ALD cycle with a TMA pulse of 360 ms on TiOPc/HOPG at 373 K, AlO_x appears as a cluster on each unit cell, without noticeable pinholes. The inset FT in Figure 2c shows only a bright contour around the center indicating an amorphous structure for AlO_x/TiOPc/HOPG. The monolayer of AlO_x appears as a nearly continuous film with no discernible pinholes in the STM images. This coverage indicates that the TMA reacts with each TiOPc molecule, and further addition of H_2O induces transformation of the adsorbates to AlO_x.

Scanning tunneling spectroscopy (STS) was employed to determine the transitions in electronic structure induced by sequential ALD pulses, as shown in Figure 2d. A variable tip−surface STS method was employed to collect a larger tunneling signal during STS measurements.[39] The TiOPc monolayer on HOPG has a band gap of about 1.7 eV and an almost symmetric density of states (DOS). After exposing TiOPc to TMA, the DOS in the valence and conduction bands significantly decreased and the band gap increased to about 2.5 eV. However, in the right, expanded STS of Figure 2d, two band gap states (s1 and s2) still remain at −0.5 and −1.2 V, which are below the E_F, indicating charge trapping in DMA/TiOPc/graphene. DFT was used to model possible charge movements as shown in Figure 2e,f. A simplified DFT model is employed in which the TMA dissociatively chemisorbs as DMA at the O atom of TiOPc/graphene because this is the strongest chemisorption site for the simplest TMA dissociation product, as discussed in the Supporting Information (Figure S9). As DMA reacts with the central O of TiOPc, a large change in the DFT PDOS of DMA/TiOPc is observed. The new states are generated near the Fermi level at −0.1 and +0.75 eV (red bars and arrows), while there is a decrease of preexisting states at −1 and +0.35 eV (blue bars and arrows). Therefore, this transition of DOS in DMA/TiOPc is consistent with the experimental observation of trap states below the Fermi level, as shown in the STS measurements. In STS, these band gap states are diminished by the following H_2O pulse. After one cycle of ALD at 373 K, the band gap increased to about 3.4 eV, and most of the states within the band gap are removed.

DFT calculations suggest the existence of multiple stable binding sites (O, N, and C) for DMA on TiOPc molecules, which is required for high nucleation density after one ALD cycle as shown in Figures S9 and S11; all sites can bond DMA at 373 K to convert into AlO_x during ALD. Combining STM images of Figure 2, a simplified model is proposed in Figure 2g. Initially, TMA dissociates into DMA and chemisorbs onto TiOPc, bonding to O, N, or C sites at 373 K. Therefore, multiple DMA molecules coexist on each TiOPc molecule after the first TMA pulse. Subsequently, the H_2O pulse transforms the $Al(CH_3)_2$ into $Al(OH)_2$ and induces cross-linking of Al−O−Al similar to what is observed on Si(100).[35] Finally, after exposing the TiOPc/HOPG to multiple cycles of ALD, AlO_x begins to grow between the TiOPc molecules, consistent with the AFM images in Figures 2h and S13.

The deposition of a subnanometer dielectric on TiOPc/HOPG significantly decreases the surface tunneling conductance between the STM tip and the sample. A schematic of the tunneling junction between the metal STM tip and AlO_x/TiOPc/HOPG is displayed in Figure 3a. The tunneling current measured as a function of sample bias for both TiOPc/HOPG and ALD deposited TiOPc/HOPG (one and five ALD cycles) are shown in Figure 3b, and nine different STS IV curves after one and five cycles of ALD are included in Figure 3c. For TiOPc/HOPG, an increasing current is measured for both positive and negative sample biases, producing a V-shaped $I-V$ plot with high currents. In contrast, after one cycle of TMA/H_2O, the tunneling current decreases throughout the bias range by more than 1 order of magnitude compared to the bare TiOPc/HOPG, while the offset position is shifted to a positive bias. The reduced tunneling current is attributed to the energy barrier introduced by the subnanometer AlO_x layer, resulting in a decreased probability of tunneling electrons, as depicted in Figure 3d. It is noted that the shift of the offset bias in STS results from trap or fixed charge states in dielectric or at the interface of dielectric−TiOPc because these dielectrics were processed without postdeposition annealing. Therefore, it is

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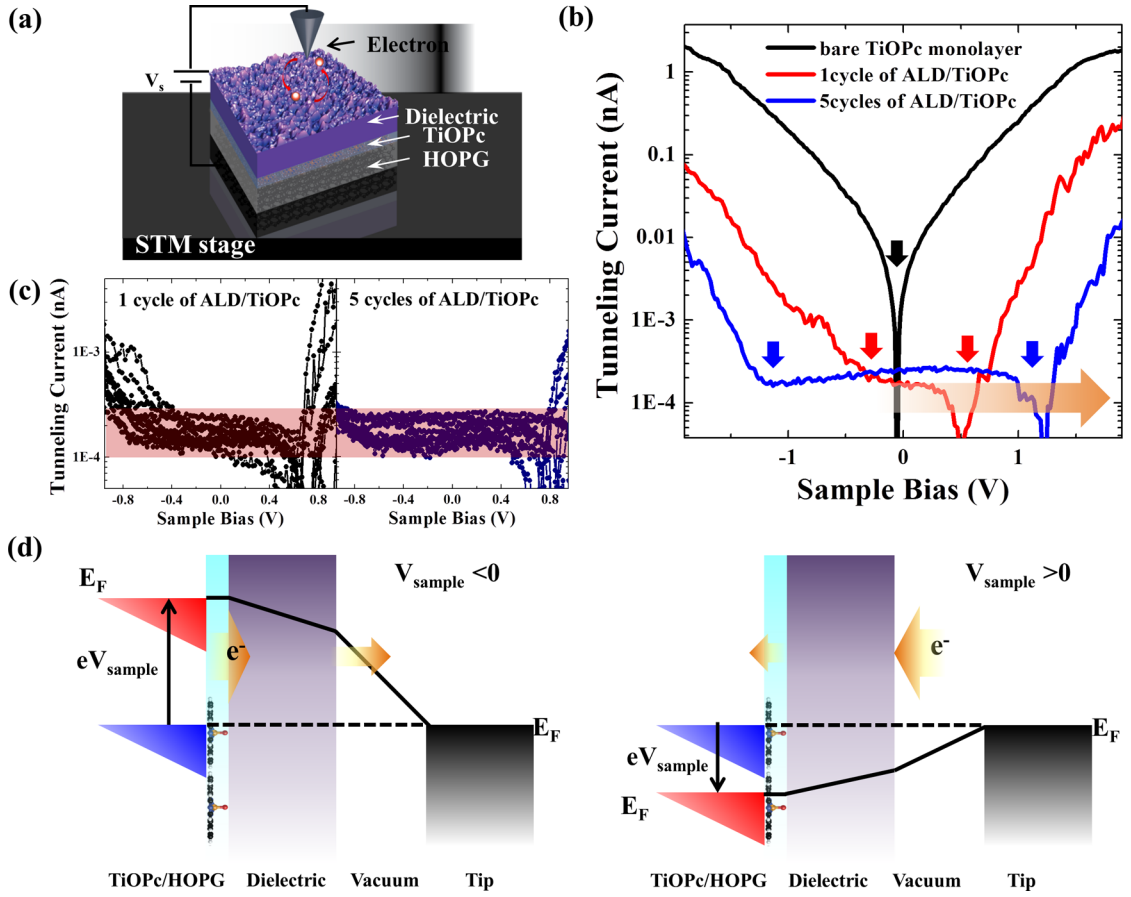

Figure 3. Scanning tunneling characterization of deposited subnanometer dielectric layers. (a) Schematic of tunnel junction in metal tip/vacuum/AlO_x(purple)/TiOPc(sky blue)/HOPG(gray) on the STM stage. (b) Log scaled tunneling current of a TiOPc monolayer, AlO_x deposited by one and five cycles of TMA/H_2O pulses on TiOPc/HOPG. All STS were taken by sweeping from negative to positive bias. (c) Nine different STS IV curves taken after one and five cycles of ALD/TiOPc/HOPG. (d) Simplified model of tunneling conductance through deposited subnanometer dielectric under negative (left) and positive (right) sample bias. Electrostatic potential profiling modulated by sample bias is shown as black solid line.

possible there are excess oxygen or defects states in dielectric, as shown in Figure S14.[37,38] The tunneling current further decreases by an order of magnitude after 5-cycles of ALD in Figure 3b. In this case, the low current regime expands to a larger voltage range. As the thickness of the insulating dielectric increased due to additional ALD cycles on TiOPc/HOPG, increasing the tunnel barrier width, the tunneling of charge carriers from the metal tip (sample) to sample (tip) requires applying higher bias thereby the onset bias is pushed to a higher voltage range, as shown by an orange arrow in Figure 3b. This shift of onset bias is more prominently shown in the nine different IV curves taken after one and five cycles ALD/TiOPc/HOPG in Figure 3c. It is noted that although the current of one cycle ALD/TiOPc/HOPG (1.4×10^{-4} to 1.87×10^{-4} nA) is slightly lower in the flat regions of the $I-V$ curves than the current of five cycles ALD/TiOPc/HOPG (1.5×10^{-4} to 2.5×10^{-4} nA) in Figure 3b, the current levels of both samples are very low in the flat regions of the $I-V$ curves; therefore, this difference is within the noise level of the measurement. As shown in Figure 3c, both one and five cycles ALD/TiOPc/HOPG possess the similar variation of current levels (from 1×10^{-4} to 3×10^{-4} nA) in the flat region of the $I-V$ curves as displayed by the red bars.

Figure 4a shows the schematic of Ni/AlO_x/TiOPc/graphene capacitors fabricated on SiO_2/Si, with 50 cycles of ALD. The V-shape of the CV curves in Figure 4b is due to the effect of the quantum capacitance of graphene.[40,41] CV curves with variable frequencies (from 1 kHz to 1 MHz) are included in Figure S15 of the Supporting Information. Previous reports have mostly employed thick dielectric layers (8−20 nm) to measure CV due to limitations imposed by large pinhole densities in thin layers.[27] However, since the AlO_x/TiOPc/graphene has a very low pinhole density compared to previous reports, thinner capacitors could be fabricated even with conventional thermal metal gate deposition. At −3 V, the maximum capacitance (C_{max}) is over 1000 nF/cm^2 at 1 kHz, which is larger than prior reported values on graphene.[25,27,28] Instead C_{max} reported here is consistent with InGaAs with 4.7 nm of Al_2O_3.[42] The contact resistance between graphene and the Au contact is manifest by the difference of C_{max} between 1 and 2 kHz.[43,44] Moreover, near zero capacitance is observed at 0 V, which results from low minority carriers at the interface, indicating the full modulated capacitance by gate bias. The leakage current in the capacitor is shown in Figure 4c to be around 0.02 A/cm^2 at a gate bias of ±3 V. As shown below, small area devices have a lower leakage current per unit area, which is consistent with leakage being limited by particulate-induced pinholes resulting from graphene grain boundaries.[45]

To further evaluate the quality of the 4 nm dielectric, dual-gated, exfoliated graphene FETs were fabricated as shown in Figure 4d. In this case, 40 cycles of AlO_x/TiOPc were deposited. A Ni top gate was deposited on AlO_x/TiOPc/

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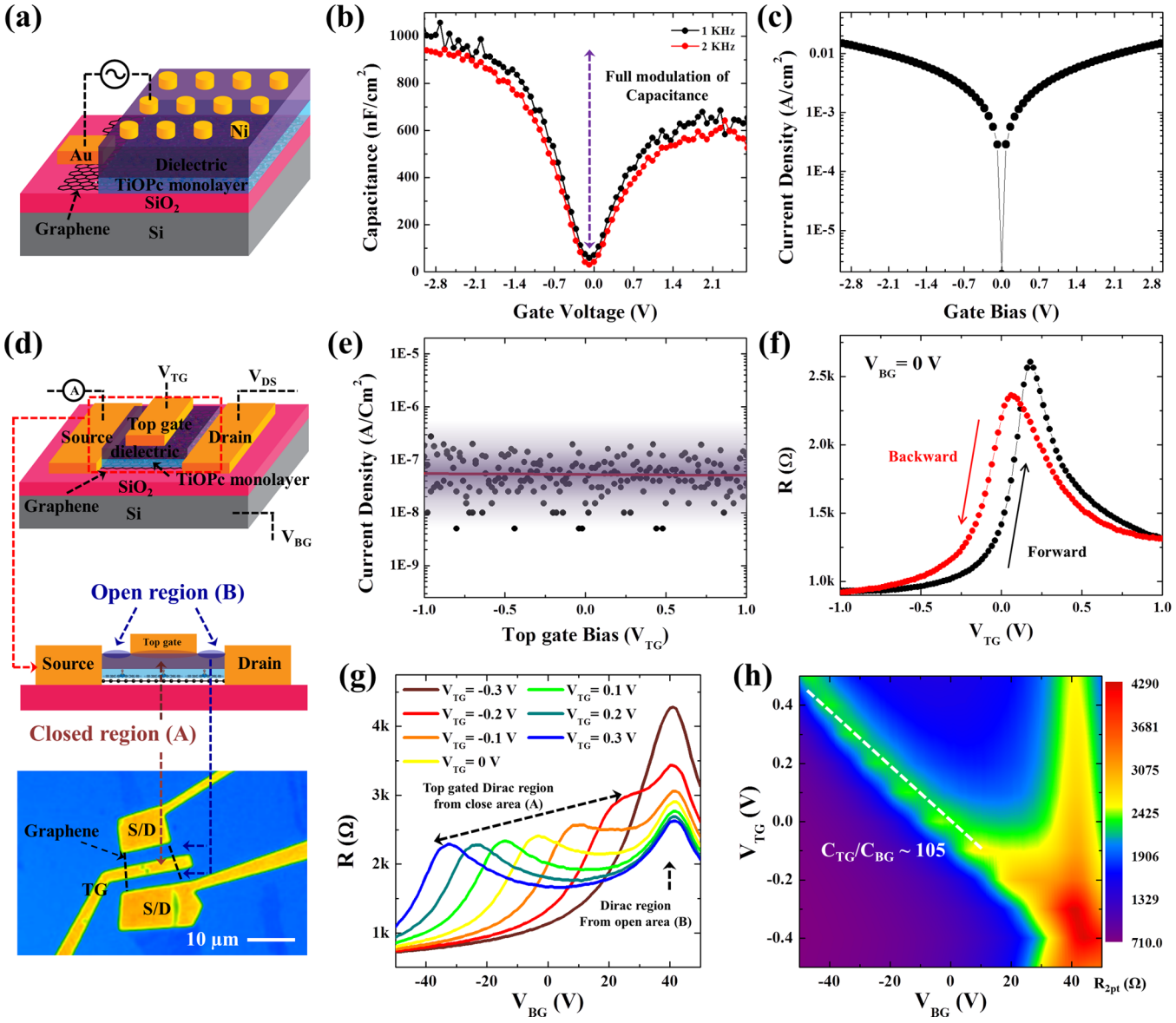

Figure 4. Electrical characterization of deposited ~4 nm dielectric layer. (a) Schematic of metal−oxide−graphene capacitor with TiOPc seed monolayer. (b) Capacitance−voltage data for 50 ALD cycle dielectric layer on TiOPc/graphene/SiO_2/Si. (c) Leakage current density−voltage data of same capacitor; IV reported at 1 MHz. (d) Schematic of dual gate 40 cycles dielectric-graphene FET and corresponding optical image. (e) Leakage current density-top gate bias of graphene FET. (f) Resistance versus top gate bias at 0 V back gate bias. The hysteresis between forward and backward sweeps is 0.12 V. (g) Resistance versus back gate bias at different top gate bias from −0.3 to 0.3 V. (h) Two-dimensional resistance plot as a function of top-gate voltage and back-gate voltage for a graphene FET.

graphene/SiO_2/Si, and a highly N-doped Si substrate was used as a back gate, allowing dual-gate control of the carrier concentration in graphene. The leakage current of the FET is below 10^{-7}A/cm^2 within a top gate bias range of −1 to +1 V, as shown in Figure 4e. This leakage current is much smaller than previous leakage values in thicker ALD-deposited Al_2O_3 on graphene (previous leakage value: about 2.2×10^{-6} A/cm^2 in 4.5 nm Al_2O_3 and 1.9×10^{-7} A/cm^2 in 15 nm Al_2O_3).[26,46] The resistance is measured at V_{BG} = 0 V over a top gate range of ±1 V in Figure 4f. The position of maximum resistance (Dirac point) of the device is at V_{TG} = 0.17 V for the forward sweep, while the reverse sweep shifts the Dirac point to 0.05 V, giving rise to a 0.12 V hysteresis. Compared to previous reports, the positions of the Dirac points are closer to 0 V and the hysteresis is smaller[3,26,46] suggesting the TiOPc seed layer and subsequent dielectric deposition does not induce a significant amount of chemical doping or interfacial trap defects. Integrating of TiOPc seedling layer into ALD process, the MoS_2-ALD dielectric-TiOPc-graphene interlayer device also was fabricated and characterized, as displayed in Figure S16.

Figure 4g shows resistance as a function of back gate bias (−50 to 50 V) for varying top gate biases in the range of −0.3 to 0.3 V. From the device schematic in Figure 4d, it can be seen that while the back-gate can modulate the entire graphene channel, the top-gate can only modulate the local channel region under the top-gate. Therefore, the modulation of the top and bottom gates induce shifts of Dirac point originating from the graphene channel, as shown in Figure 4g. As V_{TG} is varied, the carrier density in the top-gated region changes and can be neutralized by applying an appropriate V_{BG}.[26,47] At 0, V_{TG} are detected: one at V_{Bg} = 0 V, which is the primary Dirac point, and a second at $V_{Bg} \approx$ 40 V. These two "Dirac points" results

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from the coexistence of a top gated dielectric/graphene region (A) and an open dielectric/graphene region (B) as shown in Figure 4d. Since only region A is affected by the top-gate, the primary Dirac point corresponding to this region would shift when the top-gate voltage is changed, while the secondary Dirac point remains at 40 V. At V_{TG} = −0.3 V, the large peak located at V_{BG} = 40 V is when the top-gate is biased in such a way that the primary Dirac point overlaps with the secondary Dirac point and causes a "series addition" of the two resistances, leading to a large peak, which appears as a single Dirac point.

Figure 4h shows a two-dimensional plot of the channel resistance as a function of the back-gate bias (V_{BG}), and top-gate bias (V_{TG}). The variation of both Primary and Secondary Dirac point is displayed in Figure 4h. The slope along the variation of Primary Dirac points represents the ratio of capacitances of the top-gate and back-gate as shown dashed line. From the slope of the V_{BG} vs V_{TG} for channel resistance (Figure 4h), the capacitance ratio is calculated as 105 from the equation slope = V_{TG}/V_{BG} = C_{TG}/C_{BG}. The back-gate capacitance is ∼11 nF/cm^2 for a 300 nm back-gate SiO_2 oxide; therefore, the top-gate capacitance is calculated as 1155 nF/cm^2.

The deposition of a dielectric layer with a high nucleation density was demonstrated by using a TiOPc seed layer prior to ALD. *In situ* STM was employed to image each step of the process with molecular resolution. The TiOPc layer has long-range order and shows high reactivity with TMA; after exposure to TMA for 70 ms at 373 K, TMA dissociatively chemisorbs on TiOPc/HOPG resulting in multiple chemisorption sites. After exposure to 1 cycle ALD pulse, the high coverage of AlO_x is obtained without noticeable pinholes. STS measurements show that one cycle of ALD on TiOPc/HOPG increases the band gap from 1.7 to 3.4 eV, while the tunneling current is decreased by one order of magnitude. These results are consistent with the formation of a subnanometer oxide. DFT calculations show that O, N, and C sites of the TiOPc molecules have high binding energy with DMA, consistent with the existence of multiple reaction sites per single TiOPc molecule. With capacitor and dual-gated devices, the dielectric shows insulating properties with high-quality CV and RV characteristics. The combination of high-quality subnanometer dielectric deposition and *in situ* measurements provides a pathway for large-scale fabrication of 2D interlayer devices, which can be extended to other 2D crystals and devices.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b02429.

Experimental details and methods (ALD, STS, growth of graphene, DFT, and fabrication of capacitors and devices), TiOPc molecular structure, and AFM images (PDF)

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: akummel@ucsd.edu.

Author Contributions

J.H.P and A.C.K conceived and designed this experiment. J.H.P. performed STM experiments. J.H.P and A.C.K analyzed the STM/STS data. E.C. and P.C. performed DFT calculations, and A.C.K. reviewed the calculations. ALD process was performed by I.K., K.S., and K.H. I.K. performed AFM. Growth of graphene and transfer was performed by H.C.P. and H.C. Graphene capacitor fabrication was performed by K.H. and K.S. Dual gated graphene devices were fabricated by H.C.P. CV was measured by K.S., K.H., and H.C.P. All data was discussed by J.H.P., S.F., S.B., and A.C.K. J.H.P. wrote most of manuscript.

Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. *Science* **2004**, *306*, 666−669.

(2) Geim, A. K.; Novoselov, K. S. *Nat. Mater.* **2007**, *6*, 183−191.

(3) Meric, I.; Han, M. Y.; Young, A. F.; Ozyilmaz, B.; Kim, P.; Shepard, K. L. *Nat. Nanotechnol.* **2008**, *3*, 654−659.

(4) Williams, J. R.; DiCarlo, L.; Marcus, C. M. *Science* **2007**, *317*, 638−641.

(5) Seabaugh, A. C.; Zhang, Q. *Proc. IEEE* **2010**, *98*, 2095−2110.

(6) Banerjee, S. K.; Register, L. F.; Tutuc, E.; Reddy, D.; MacDonald, A. H. *IEEE Electron Device Lett.* **2009**, *30*, 158−160.

(7) Reddy, D.; Register, L. F.; Tutuc, E.; Banerjee, S. K. *IEEE Trans. Electron Devices* **2010**, *57*, 755−764.

(8) Britnell, L.; Gorbachev, R. V.; Jalil, R.; Belle, B. D.; Schedin, F.; Katsnelson, M. I.; Eaves, L.; Morozov, S. V.; Mayorov, A. S.; Peres, N. M. R.; Neto, A. H. C.; Leist, J.; Geim, A. K.; Ponomarenko, L. A.; Novoselov, K. S. *Nano Lett.* **2012**, *12*, 1707−1710.

(9) Britnell, L.; Gorbachev, R. V.; Jalil, R.; Belle, B. D.; Schedin, F.; Mishchenko, A.; Georgiou, T.; Katsnelson, M. I.; Eaves, L.; Morozov, S. V.; Peres, N. M. R.; Leist, J.; Geim, A. K.; Novoselov, K. S.; Ponomarenko, L. A. *Science* **2012**, *335*, 947−950.

(10) Feenstra, R. M.; Jena, D.; Gu, G. *J. Appl. Phys.* **2012**, *111*, 043711.

(11) Britnell, L.; Gorbachev, R. V.; Geim, A. K.; Ponomarenko, L. A.; Mishchenko, A.; Greenaway, M. T.; Fromhold, T. M.; Novoselov, K. S.; Eaves, L. *Nat. Commun.* **2013**, *4*, 1794.

(12) Roy, T.; Hesabi, Z. R.; Joiner, C. A.; Fujimoto, A.; Vogel, E. M. *Microelectron. Eng.* **2013**, *109*, 117−119.

(13) Zhao, P.; Feenstra, R. M.; Gu, G.; Jena, D. *IEEE Trans. Electron Devices* **2013**, *60*, 951−957.

(14) Roy, T.; Liu, L.; de la Barrera, S.; Chakrabarti, B.; Hesabi, Z. R.; Joiner, C. A.; Feenstra, R. M.; Gu, G.; Vogel, E. M. *Appl. Phys. Lett.* **2014**, *104*, 123506.

(15) Li, M.; Esseni, D.; Snider, G.; Jena, D.; Xing, H. G. *J. Appl. Phys.* **2014**, *115*, 074508.

(16) Fogler, M. M.; Butov, L. V.; Novoselov, K. S. *Nat. Commun.* **2014**, *5*, 4555.

(17) Gilbert, M. J. *IEEE Trans. Electron Devices* **2010**, *57*, 3059−3067.

(18) Mishchenko, A.; Tu, J. S.; Cao, Y.; Gorbachev, R. V.; Wallbank, J. R.; Greenaway, M. T.; Morozov, V. E.; Morozov, S. V.; Zhu, M. J.; Wong, S. L.; Withers, F.; Woods, C. R.; Kim, Y. J.; Watanabe, K.; Taniguchi, T.; Vdovin, E. E.; Makarovsky, O.; Fromhold, T. M.; Fal'ko,

DOI: 10.1021/acs.nanolett.5b02429
Nano Lett. 2015, 15, 6626−6633

V. I.; Geim, A. K.; Eaves, L.; Novoselov, K. S. *Nat. Nanotechnol.* **2014**, *9*, 808−813.
(19) Khorasani, S. A. *IEEE J. Quantum Electron.* **2014**, *50*, 307−313.
(20) Fallahazad, B.; Lee, K.; Kang, S.; Xue, J. M.; Larentis, S.; Corbet, C.; Kim, K.; Movva, H. C. P.; Taniguchi, T.; Watanabe, K.; Register, L. F.; Banerjee, S. K.; Tutuc, E. *Nano Lett.* **2015**, *15*, 428−433.
(21) Kim, S.; Jo, I.; Nah, J.; Yao, Z.; Banerjee, S. K.; Tutuc, E. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2011**, *83*, 161401.
(22) Kim, S.; Jo, I.; Dillen, D. C.; Ferrer, D. A.; Fallahazad, B.; Yao, Z.; Banerjee, S. K.; Tutuc, E. *Phys. Rev. Lett.* **2012**, *108*, 116404.
(23) Xuan, Y.; Wu, Y. Q.; Shen, T.; Qi, M.; Capano, M. A.; Cooper, J. A.; Ye, P. D. *Appl. Phys. Lett.* **2008**, *92*, 013101.
(24) Liao, L.; Duan, X. F. *Mater. Sci. Eng., R* **2010**, *70*, 354−370.
(25) Alaboson, J. M. P.; Wang, Q. H.; Emery, J. D.; Lipson, A. L.; Bedzyk, M. J.; Elam, J. W.; Pellin, M. J.; Hersam, M. C. *ACS Nano* **2011**, *5*, 5223−5232.
(26) Jandhyala, S.; Mordi, G.; Lee, B.; Lee, G.; Floresca, C.; Cha, P. R.; Ahn, J.; Wallace, R. M.; Chabal, Y. J.; Kim, M. J.; Colombo, L.; Cho, K.; Kim, J. *ACS Nano* **2012**, *6*, 2722−2730.
(27) Sangwan, V. K.; Jariwala, D.; Filippone, S. A.; Karmel, H. J.; Johns, J. E.; Alaboson, J. M. P.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C. *Nano Lett.* **2013**, *13*, 1162−1167.
(28) Shin, W. C.; Bong, J. H.; Choi, S. Y.; Cho, B. J. *ACS Appl. Mater. Interfaces* **2013**, *5*, 11515−11519.
(29) Terrones, M.; Botello-Mendez, A. R.; Campos-Delgado, J.; Lopez-Urias, F.; Vega-Cantu, Y. I.; Rodriguez-Macias, F. J.; Elias, A. L.; Munoz-Sandoval, E.; Cano-Marquez, A. G.; Charlier, J. C.; Terrones, H. *Nano Today* **2010**, *5*, 351−372.
(30) McDonnell, S.; Brennan, B.; Azcatl, A.; Lu, N.; Dong, H.; Buie, C.; Kim, J.; Hinkle, C. L.; Kim, M. J.; Wallace, R. M. *ACS Nano* **2013**, *7*, 10354−10361.
(31) Dlubak, B.; Seneor, P.; Anane, A.; Barraud, C.; Deranlot, C.; Deneuve, D.; Servet, B.; Mattana, R.; Petroff, F.; Fert, A. *Appl. Phys. Lett.* **2010**, *97*, 092502.
(32) Martin, M. B.; Dlubak, B.; Weatherup, R. S.; Yang, H.; Deranlot, C.; Bouzehouane, K.; Petroff, F.; Anane, A.; Hofmann, S.; Robertson, J.; Fert, A.; Seneor, P. *ACS Nano* **2014**, *8*, 7890−7895.
(33) Liu, H.; Xu, K.; Zhang, X. J.; Ye, P. D. *Appl. Phys. Lett.* **2012**, *100*, 152115.
(34) Norton, J. E.; Bredas, J. L. *J. Chem. Phys.* **2008**, *128*, 034701.
(35) Dillon, A. C.; Ott, A. W.; Way, J. D.; George, S. M. *Surf. Sci.* **1995**, *322*, 230−242.
(36) Potts, S. E.; Profijt, H. B.; Roelofs, R.; Kessels, W. M. M. *Chem. Vap. Deposition* **2013**, *19*, 125−133.
(37) Scherer, H.; Weimann, T.; Zorin, A. B.; Niemeyer, J. *J. Appl. Phys.* **2001**, *90*, 2528−2532.
(38) Hu, J.; Nainani, A.; Sun, Y.; Saraswat, K. C.; Wong, H. S. P. *Appl. Phys. Lett.* **2011**, *99*, 252104.
(39) Feenstra, R. M.; Lee, J. Y.; Kang, M. H.; Meyer, G.; Rieder, K. H. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2006**, *73*, 035310.
(40) Xia, J. L.; Chen, F.; Li, J. H.; Tao, N. J. *Nat. Nanotechnol.* **2009**, *4*, 505−509.
(41) Xia, J. L.; Chen, F.; Tedesco, J. L.; Gaskill, D. K.; Myers-Ward, R. L.; Eddy, C. R.; Ferry, D. K.; Tao, N. J. *Appl. Phys. Lett.* **2010**, *96*, 162101.
(42) Kim, E. J.; Chagarov, E.; Cagnon, J.; Yuan, Y.; Kummel, A. C.; Asbeck, P. M.; Stemmer, S.; Saraswat, K. C.; McIntyre, P. C. *J. Appl. Phys.* **2009**, *106*, 124508.
(43) Russo, S.; Craciun, M. F.; Yamamoto, M.; Morpurgo, A. F.; Tarucha, S. *Phys. E* **2010**, *42*, 677−679.
(44) Xia, F. N.; Perebeinos, V.; Lin, Y. M.; Wu, Y. Q.; Avouris, P. *Nat. Nanotechnol.* **2011**, *6*, 179−184.
(45) Li, X. S.; Cai, W. W.; An, J. H.; Kim, S.; Nah, J.; Yang, D. X.; Piner, R.; Velamakanni, A.; Jung, I.; Tutuc, E.; Banerjee, S. K.; Colombo, L.; Ruoff, R. S. *Science* **2009**, *324*, 1312−1314.
(46) Lee, B.; Mordi, G.; Kim, M. J.; Chabal, Y. J.; Vogel, E. M.; Wallace, R. M.; Cho, K. J.; Colombo, L.; Kim, J. *Appl. Phys. Lett.* **2010**, *97*, 043107.
(47) Kim, S.; Nah, J.; Jo, I.; Shahrjerdi, D.; Colombo, L.; Yao, Z.; Tutuc, E.; Banerjee, S. K. *Appl. Phys. Lett.* **2009**, *94*, 062107.

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Nano Lett. 2015, 15, 6626−6633