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The influence of surface preparation on low temperature HfO₂ ALD on InGaAs (001) and (110) surfaces

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Current logic devices rely on 3D architectures, such as the tri-gate field effect transistor (finFET), which utilize the (001) and (110) crystal faces simultaneously thus requiring passivation methods for the (110) face in order to ensure a pristine 3D surface prior to further processing. Scanning tunneling microscopy (STM), x-ray photoelectron spectroscopy (XPS), and correlated electrical measurement on MOSCAPs were utilized to compare the effects of a previously developed in situ pre-atomic layer deposition (ALD) surface clean on the InGaAs (001) and (110) surfaces. Ex situ wet cleans are very effective on the (001) surface but not the (110) surface. Capacitance voltage indicated the (001) surface with no buffered oxide etch had a higher C_{max} hypothesized to be a result of poor nucleation of HfO₂ on the native oxide. An *in situ* pre-ALD surface clean employing both atomic H and trimethylaluminum (TMA) pre-pulsing, developed by Chobpattana et al. and Carter et al. for the (001) surface, was demonstrated to be effective on the (110) surface for producing low D_{it} high C_{ox} MOSCAPs. Including TMA in the pre-ALD surface clean resulted in reduction of the magnitude of the interface state capacitance. The XPS studies show the role of atomic H pre-pulsing is to remove both carbon and oxygen while STM shows the role of TMA pre-pulsing is to eliminate H induced etching. Devices fabricated at 120 °C and 300 °C were compared. © 2015 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4934656]

INTRODUCTION

A few of the major obstacles facing III-V based transistors is the increased power dissipation that results from subthreshold leakage current, band to band tunneling, and aggressive gate oxide scaling.^{1,2} Tunneling through the gate oxide exhibits an exponential dependence on oxide thickness, and scaling dielectric below 1 nm equivalent oxide thickness (EOT) results in unacceptable leakage currents.^{3,4} In order to minimize gate leakage, without sacrificing capacitance, high-k materials can be employed. This allows for a physically thicker oxide and equal or higher capacitances than for traditional SiO₂ dielectrics.^{5–8} Utilizing high-k materials such as HfO₂ and Al₂O₃ has already allowed for EOT below 1 nm and devices that outperform traditional Si based metal oxide semiconductor field effect transistors (MOSFETs).9,10 This work focuses on deposition of high-k on III-V channels; to continue aggressively scaling the gate oxide on III-V's it is crucial to maximize the nucleation density of the high-k atomic layer deposition (ALD) precursors so that the dielectric film closes to form a continuous film on the substrate in a small number of ALD cycles.

Compound semiconductor based MOS devices also suffer from a relatively high density of interface trap states (D_{it}) at the semiconductor/high-k interface. These electronic trap states result from physical defects at the interface such as dangling bonds, metallic bonds, strained bonds, and defective native oxides. These can result directly from poor initiation of high-k ALD on the semiconductor surface.^{11–13} To increase drive current and minimize power consumption of III-V devices, it is important to minimize the D_{it} . Subcutaneous oxidation of the substrate and plasma induced damage during pre-ALD surface cleans can also generate D_{it} . It is possible to utilize hydrogen to remove native oxide as demonstrated by Melitz *et al.*¹⁴ and Carter *et al.*,¹⁵ and Chobpattana *et al.*,¹⁶ demonstrated that by utilizing trimethylaluminum (TMA) and H₂ plasma prior to ALD of Al₂O₃ and HfO₂ capacitance voltage (CV) characteristics can be improved at 300 °C.¹⁷

In this study, a pre-ALD *ex situ* wet clean and *in situ* dry etch were examined on both InGaAs (001) and InGaAs (110) surfaces in order to determine their effects on the nucleation of HfO₂ during ALD at 120 °C. The different surface reconstructions result not only in different Fermi level pinning behavior but also in varying degrees of nucleation for HfO₂ and thus interface trap density. In the absence of TMA in the process, low ALD temperature is of interest in order to minimize hydrogen plasma damage of both the (001) and (110) surfaces and to limit subcutaneous oxidation of the substrate by H₂O and O₂, both of which can diffuse through HfO₂.¹⁸ Scanning tunneling microscopy was used to gain an atomic level understanding of the processes occurring during the

in situ clean. X-ray photoelectron spectroscopy (XPS) and CV analysis were used to determine the effect of a buffered oxide etch (BOE) on the nucleation of HfO₂.

EXPERIMENTAL

MOSCAPs were fabricated with 300 nm of InGaAs (001) grown by molecular beam epitaxy (MBE) with 1×10^{17} cm⁻³ Si doping on n-type InP (001) substrates. The InGaAs (110) samples were grown by MBE with 1×10^{17} cm⁻³ Si doping on InP (110) substrates. MOSCAP samples were initially degreased for 3 min in acetone, isopropyl alcohol (IPA), and deionized (DI) water. Immediately prior to loading samples into the ALD chamber, for some samples, the native oxide was removed with a 3 min dip in a BOE solution comprised of a 30:4 ratio of 36% NH₄F and 8% HF followed by a 1 min rinse in DI water. Samples were quickly loaded (1-2 min air exposure) into an Oxford Instruments FlexAL ALD reactor equipped with a remote plasma source which enables low temperature ALD and minimizes surface damage. Some samples received an in situ surface clean prior to ALD consisting of a 20 mTorr inductively coupled 100 W H₂ plasma for 2 s, 40 ms of 200 mTorr TMA, and another H₂ plasma pulse. For some experiments, the TMA pulse was eliminated.^{15,16} For samples deposited with HfO2 at 120 °C, an ALD cycle consisted of a 1 s pulse of 80 mTorr tetrakis(ethylmethylamino)hafnium (TEMAH), a 7 s Ar purge, a 1 s 80 mTorr H₂O pulse, and a 35 s purge. For samples deposited with HfO₂ at 300 °C a 1 s 80 mTorr pulse of TEMAH, 5 s Ar purge, 5 s pump, 0.05 s 80 mTorr H₂O pulse 7 s Ar purge, and 7 s pump were employed. All samples underwent a 15 min 400 °C forming gas anneal (FGA, 5% H₂, 95% N₂) prior to metal deposition. The gate metal was 50 nm thick thermally evaporated Ni deposited in 150 μ m diameter circular electrodes using a shadow mask. Thermal evaporation was utilized since previous work has shown ebeam evaporation can increase Dit. The backside contact was a blanket deposited 20 nm thick thermally evaporated Ni film coated by 80 nm of thermally evaporated Au. CV, IV curves were measured using a HP4284A LCR meter and an Agilent B1500 Semiconductor Device Analyzer. The frequency range of all CV measurements is from 1 kHz (blue) to 1 MHz (grey). All Dit values were calculated using the full interface state model.¹⁹ At least 10 CV measurements were performed on separate gates for each sample to ensure uniformity across the sample.

InGaAs (001) samples used for scanning tunneling microscopy (STM) were grown by MBE with 1×10^{18} cm⁻³ Si doping on InP (001) substrates and were capped with 50 nm of As₂. Samples were loaded into a variable temperature Omicron ultrahigh vacuum chamber and the As₂ cap was removed by heating the samples to 350 °C for 30 min and the (2 × 4) reconstruction was obtained by heating to 400 °C for at least 30 min. Details of the (2 × 4) reconstruction are given elsewhere.^{20,21} Samples were subsequently exposed to atomic H generated from an Oxford Applied Research TC-50 thermal gas cracker. The hydrogen doses are reported in Langmuir (1 L = 1 s at 1 × 10⁻⁶ Torr) based on the H₂ pressure; however, the cracking efficiency is reported to be closer to 50% (Oxford Applied Research) but could not be verified; therefore, the reported atomic

H doses are an upper limit. Various amounts of TMA were also deposited on the samples; details of specific dose amounts of atomic H and TMA are given in the section titled "Results and Discussion." After dosing, samples were transferred to the scanning probe microscopy (SPM) chamber, base pressure $\sim 1 \times 10^{-11}$ Torr. STM was performed using a tunneling current set point of 100 pA and a constant tip-sample bias of -3.0 V. All STM images were reproduced at least twice. XPS was performed with a monochromatic XM 1000 MkII/Sphera system developed by Omicron Nanotechnology. A constant analyzer pass energy of 50 eV was employed with a 0.1 eV linewidth obtained using a monochromatic Al K α source (1486.7 eV). The takeoff angle was 30° relative to the surface (surface sensitive) with an acceptance angle of 7°. All spectra were analyzed with CASA XPS v. 2.3. An assumption made in this study is that the majority of reactive species created in the plasma are atomic H and thus using a thermal atomic H source for XPS and STM studies is a valid comparison. The thermally generated atomic H was at 1×10^{-6} Torr while the H plasma was at 0.02 Torr so plasma induced damaged in CV due to atomic H would be, if anything, lower than the damage you would expect from thermally generated atomic H.

RESULTS AND DISCUSSION

In situ native oxide/contaminant removal

Capacitance voltage profiling is an effective way to both qualitatively determine the quality of the oxide and quantitatively determine the trap density at the semiconductor/oxide interface (D_{it}) and the border trap density in the oxide (N_{bt}). For n-type samples at positive gate biases >1 V, electrons accumulate at the surface of the InGaAs and the measured capacitance is a reflection of the thickness and quality of the oxide.

The dispersion with frequency upon sweeping the gate bias toward accumulation reflects the density of border traps (N_{bt}) in the absence of series (e.g., contact) resistance. The border trap response is frequency dependent because the time constant for filling and emptying the traps depends on their depth and energy distributions in the oxide. The magnitude of the accumulation dispersion with frequency gives a qualitative description of the N_{bt} and, when more thorough modeling techniques are used, this dispersion can contribute to the quantification of N_{bt} .

As the gate bias is swept toward inversion, a "false inversion bump" is frequently observed for III-V substrates. This is a result of charges being injected into electronic trap states at the interface (D_{it}), rather than true inversion. When sweeping the bias outside of the energy range of the traps, or when the measurement frequency and/or temperature is too low to detect the capacitive signature of the traps, this trap capacitance subsides. The magnitude of the false inversion bump gives a qualitative description of the D_{it} and, when more thorough modeling techniques are used, this bump can contribute to the quantification of D_{it} .

The effect of TMA incorporation into the *in situ* pre-ALD surface clean was investigated by fabricating MOSCAPs on InGaAs (001) with 10 cycles of either H plasma alone or H/TMA/H followed by 40 cycles of HfO₂ ALD at 120 °C or



FIG. 1. (a) CV curve obtained after exposing InGaAs (001) to 10 cycles of H plasma at 300 °C prior to ALD. A large false inversion bump is observed which is attributed to the plasma damaging the InGaAs surface. (b) InGaAs sample exposed to 10 cycles of H/TMA/H prior to ALD at 300 °C. Addition of a TMA pulse dramatically reduces the magnitude of the false inversion bump suggesting it is preventing or repairing plasma damage. (c) InGaAs samples exposed to 10 cycles of H plasma only prior to ALD at 120 °C. False inversion bump is reduced by $2\times$ compared to 300 °C exposure confirming low temperature processing reduces plasma damage. (d) InGaAs sample exposed to 10 cycles of H/TMA/H prior to ALD at 120 °C. Again including TMA reduced the false inversion bump and suggested that it is crucial to reducing the density of interfacial trap states.

300 °C. The sample in Fig. 1(a) received 10 cycles of H plasma at 300 °C while Fig. 1(b) had 10 cycles of H/TMA/H at 300 °C. It is evident that the H plasma damaged the InGaAs surface, resulting in both a large false inversion bump (at negative gate bias), which is attributed to interface trap states,^{22,23} and the dispersion in the depletion regime (gate bias $\sim +0.5$ V). After incorporation of TMA into the pre-ALD clean the peak value of the interface state capacitance was reduced from 1.88 μ F/cm² to 0.5 μ F/cm² at 1 kHz, and the dispersion in depletion was reduced. This indicates that TMA exposure minimized the plasma induced damage to the surface resulting in a significant reduction in interfacial trap density. The same experiment was performed at 120 °C and the amount of plasma damage was reduced by temperature alone, Fig. 1(c), without adding TMA to the pre-ALD plasma treatment. The peak capacitance of the false inversion bump at 1 kHz for the 120 °C case was 0.93 μ F/cm² compared to 1.88 μ F/cm² for the 300 °C case, but dispersion throughout the depletion region remains. After incorporating TMA at 120 °C, the 1 kHz peak value of the interface state capacitance was further reduced to 0.59 μ F/cm² and the dispersion in the flatband region was reduced; as shown below this corresponds to approximately 25% decrease in the peak D_{it} near the conduction band (CB). It has been shown previously that utilizing atomic H, TMA, and TEMAH can remove native oxides on III-V surfaces,14,24 but this result indicates the TMA is playing an additional role in minimizing defect formation at both high and low temperatures.

STM was employed to determine the passivating mechanism of TMA in the pre-ALD surface clean. Previous work by Melitz *et al.* utilized STM to show that atomic H removes

carbon and oxygen from the surface but produces a high density of etching pits; here, the co-dosing of H and TMA was investigated to understand how the TMA prevents atomic H induced etching damage.¹⁴ Fig. 2(a) shows a 50×50 nm² STM image of the clean InGaAs (2×4) surface. Details of the clean (2×4) surface have been discussed in detail elsewhere.²⁰ After exposing the clean surface to 1800 Langmuir (L) of atomic H at 300 °C, bright sites with an average width and height of 5.79 nm and 0.4 nm are observed, Fig. 2(b). Atomic H is known to etch III-V surfaces; after native oxide removal, AsH₃ is the first species to thermally desorb.¹⁷ Previous studies have indicated Ga droplet formation can occur due to an increase in the Ga mobility as arsenic hydride species desorb.^{25,26} It is hypothesized that the clusters observed are metallic In/Ga clusters. Metallic bonds are known to induce trap states at semiconductor oxide interfaces consistent with the large false inversion bump observed in Fig. 1(a).^{27,28}

Fig. 2(c) shows the surface after an initial 10 000 L dose of TMA at 300 °C followed by a subsequent 1800 L dose of atomic H at 300 °C. The height, width, and density of the bright sites have been reduced but not eliminated. It is hypothesized that after monolayer deposition of TMA, the atomic H reacts with the dissociated methyl groups forming methane which desorbs. XPS below shows not all of the –CH₃ groups are removed; the surface is covered with Al(CH₃)_x groups which protect it from etching by blocking reaction between additional atomic H and substrate As, consistent with previous studies showing that the Al(CH₃)_x bonds to the As atoms.²⁹

To determine if TMA could further reduce atomic H induced etching defects, the clean surface was dosed with TMA, then atomic H, and a final dose of TMA, Fig. 2(d). Afterwards, the surface shows almost complete elimination of bright clusters; the surface is atomically ordered with 1.7 nm between adjacent rows (inset), and atomically flat indicated by presence of a single atomic step. This implies TMA not only prevents plasma damage but also cleans up any residual damage. A possible mechanism is the incoming TMA reacts with the In/Ga clusters, forming trimethylgallium (TMG) or trimethylindium which desorb. The vapor pressure of TMG at 25 °C is 226.58 Torr while the vapor pressure of TMA is 11.38 Torr suggesting desorption of TMG is likely.

The number of pre-ALD cycles was optimized to ensure effective removal of native oxide and surface contaminants to maximize the nucleation density of HfO₂ while minimizing plasma induced damage. Fig. 3 (top) shows InGaAs (001) samples which have received 2, 5, and 10 cycles of the H/TMA/H pre-ALD clean followed by 30 cycles of HfO₂ ALD at 300 °C. Utilizing 2 cycles of the pre-clean resulted in a Cmax at 1 kHz of 2.75 μ m/cm² which was reduced to 2.4 μ F/cm² when employing 5 or more cycles. This suggests that the nucleation density of HfO₂ after 2 cycles is lower than when using 5 cycles due to native oxide and/or contaminants remaining on the surface. The reduction in C_{max} is attributed to more efficient cleaning of the surface with increased H plasma cycles rather than AlO_x deposition from background water reacting with TMA. This results in a thinner overall oxide and, therefore, a slightly higher C_{max}. The dispersion in accumulation and the flat band regions remain similar for all cases while the false inversion bump is slightly reduced as the number of cycles



FIG. 2. (a) Clean InGaAs (2×4) surface. (b) (2×4) surface after exposure to atomic H at 300 °C. Formation of bright white clusters is observed with an average width of 5.79 nm and average height of 0.4 nm. (c) (2×4) surface initially exposed to TMA and subsequently atomic H, both at 300 °C. Density, height, and width of bright sites have been reduced. TMA may be providing alternate reaction pathways for the atomic H, such as formation and desorption of methane. (d) (2×4) surface exposed first to TMA, then atomic H, and a final dose of TMA. The white clusters are almost completely absent and the surface maintains atomic ordering (inset) and is atomically flat. This suggests TMA both prevents plasma damage as well as cleans up the remaining damage observed in (c). The TMA may react with the clusters and form volatile by products.

increases. The weak inversion frequency response of MOS capacitors is increasingly sensitive to D_{it} as the C_{max} value, indicative of the oxide capacitance, decreases.³⁰ Therefore, the smaller interface trap bumps in the inversion region seen in

Fig. 3 for increasing numbers of H/TMA/H cleaning cycles are consistent with removal of defect-inducing adsorbates on the InGaAs surface that create interfacial trap states. Additionally, despite a $5\times$ increase in H plasma exposure, no damage is



FIG. 3. (Top row) The number of pre-ALD H/TMA/H cycles was varied at 300 °C. Exposing the sample to 5 or more cycles of the pre clean results in a C_{max} of $\sim 2.4 \ \mu$ F/cm². This reduction in C_{max} compared to the 2 cycle case is attributed to an increase in nucleation density of HfO₂ which results from more efficient removal of native oxide or surface contaminants with 5 or more cycles. At 120 °C (bottom row), the C_{max} continually decreases as the number of cleaning cycles increases. This suggests that the H plasma is not effective at removing native oxide at lower temperatures; hence, more cleaning cycles are required to maximize the nucleation density of HfO₂. It is important to note that despite a 5× increase in plasma exposure at both temperatures, the false inversion bump actually decreases indicating efficient surface cleaning by the H plasma and also the importance of TMA in protecting the surface from plasma damage.

evident in the CV profile, emphasizing the protective role of TMA in the pre-ALD clean.

Performing the same experiments at 120 °C, Fig. 3 (bottom) indicates that, at lower temperatures, at least 10 H/TMA/H cycles are required to maximize the effectiveness of the plasma treatment and enhance the nucleation of HfO₂ during subsequent ALD. The C_{max} value continually decreases as the number of pre-ALD cycles increases, suggesting it is more difficult to remove oxide or contamination at low temperatures. The frequency dispersion of capacitance in accumulation and depletion shows no significant change among the samples, but the D_{it} bump in the inversion region does decrease with increasing number of cycles, as for the 300 °C ALD condition. Again, despite a 5× increase in plasma exposure, we see no evidence of plasma damage, highlighting the importance of TMA in this process. When 20 cycles are employed there is noticeable plasma damage (not shown).

Ex situ native oxide removal

Wet BOEs are routinely used to remove oxide from III-V substrates prior to processing. The effect of the BOE on both (001) and (110) surfaces and its impact on HfO₂ nucleation at 120 °C and 300 °C were studied. Fig. 4 compares (001) and (110) samples which received a BOE (left column) and did not receive a BOE (right column) at 120 °C. The wet cleaned samples were loaded into the ALD reactor with a maximum 2 min air exposure. All four samples were in the ALD reactor simultaneously to ensure identical deposition conditions, and each received 10 cycles of H/TMA/H pre-ALD surface clean and 30 cycles of HfO₂ ALD. The (001) sample which received the BOE shows a maximum capacitance at high frequency of

 $\sim 2 \ \mu F/cm^2$, whereas the sample which did not receive the BOE shows a C_{max} of ~2.6 μ F/cm². It is hypothesized that the native oxide on the non-BOE sample limits the nucleation of HfO₂ on the (001) surface. Limited nucleation would result in a thinner overall oxide and, therefore, a higher C_{max}. Additionally, the non-BOE sample shows a slightly D_{it} bump in inversion. This can be attributed to the presence of a variety of InGaAs native oxides which are known to be a source of trap states in III-V based devices.^{11,31,32} The (110) surface shows no significant difference between the wet cleaned and non-wet cleaned samples. This indicates HfO₂ is nucleating identically on both samples, suggesting the BOE is not effective on this surface or that the (110) surface has such a thin native oxide that the BOE etch is immaterial when in situ atomic H is employed, consistent with the XPS data described later in this report.

The same experiment was performed at 300 °C except the samples received 48 cycles of HfO₂ ALD to account for a lower growth rate, Fig. 5. Similar behavior was observed for the (001) InGaAs samples. The C_{max} for the non-BOE sample was 2.8 μ F/cm² compared to ~2.4 μ F/cm² for the sample which received a BOE. It is hypothesized that the HfO₂ is not nucleating as efficiently on the sample with a thicker native oxide, resulting in a thinner HfO₂ layer. The interface trap responses in the inversion region of the associated MOSCAPs are comparable, which can be attributed to the increased effectiveness of the H plasma at 300 °C. For the (110) samples, the C_{max} of the sample which did not receive a BOE is within 10% of the C_{max} of the BOE sample, and thus not material. The leakage current densities of the 300 °C samples were much higher than the 120 °C samples.³³ For example, the 120 °C InGaAs (001) and InGaAs (110) samples had about $100 \times$ lower leakage current density at +1 V relative to the



FIG. 4. InGaAs (001) samples which did (top left) and did not (top right) receive a BOE immediately prior to ALD at 120 °C. (001) sample which did not receive a BOE shows a C_{max} of about 2.6 μ F/cm² compared to 2 μ F/cm² for the no BOE sample. It is hypothesized that the HfO₂ nucleates more efficiently on the sample which was exposed to the BOE. All four samples were in the ALD reactor simultaneously to ensure identical deposition conditions. (110) samples that did (bottom left) and did not receive (bottom right) a BOE prior to ALD show nearly identical CV spectra. This suggests that the BOE is not effective on the (110) surface and emphasizes the need for an *in situ* dry etch which can clean both surfaces effectively.



FIG. 5. InGaAs (001) samples which did (top left) and did not (top right) receive a BOE immediately prior to ALD at 300 °C. (001) sample which did not receive a BOE shows a C_{max} of about 2.8 μ F/cm² compared to 2.4 μ F/cm² for the no BOE sample. It is hypothesized that the HfO₂ nucleates more efficiently on the sample which was exposed to the BOE. All 4 samples were in the ALD reactor simultaneously to ensure identical deposition conditions. The (110) sample which did not receive a BOE shows a C_{max} within 10% of the BOE sample hence any differences are immaterial.

flat band voltage (V_{fb}) than the corresponding 300 °C samples. This may be due to the presence of a small CVD component in the 120 °C ALD recipe which resulted in thicker oxides. At 120 °C, the growth rate per cycles was ~1.4 Å/cycle while at 300 °C the growth rate was closer to 1 Å/cycles, as measured by ellipsometry.

X-ray photoelectron spectroscopy

XPS was used to investigate the composition of the (001) and (110) surfaces after the BOE and during the H/TMA/H pre-ALD clean.³³ The integrated carbon and oxygen 1 s signals are normalized to the sum of the In 3d, Ga 2p, and As 3d peaks in the bar chart in Fig. 6. The red column is the initial sample, green is after the first atomic H dose, purple after a subsequent TMA dose, and blue after the final atomic H clean. The same process matrix is presented as in Figs. 4 and 5. The H/TMA/H dosing was performed at 120 °C. The as-loaded (001) samples which did not receive a BOE exhibit much higher levels of carbon and oxygen than the (001) BOE sample which is expected. The initial (110) sample which received a BOE shows a reduction in carbon compared to the non-BOE sample, but the oxygen surface composition of both the non-BOE and BOE samples is almost identical. The (110) surface is inherently more stable than the (001) surface and may be less prone to oxidation than the (001) surface due to its simple surface reconstruction.^{34,35} The ineffectiveness of the BOE to remove the oxygen on the (110) surface mirrors the similar CV curves are observed in Fig. 4. After exposing both (001) samples to 1800 L of atomic H at 120 °C (green bars), the amount of C and O is reduced to similar levels on both non-BOE and BOE samples. The (110) surface exhibited the same trend and the atomic H reduced the ratio of carbon to InGaAs to about 0.2-0.3 while the ratio of oxygen to InGaAs was

reduced to less than 0.1. It was not expected that the atomic H would remove all the surface carbon in a single dose because the cyclic H/TMA process is designed to concurrently remove carbon bonded to InGaAs while protecting the surface dosed with TMA which has carbon bonded to Al. As shown in purple bars in Fig. 6, all samples show an increase in carbon after a subsequent 10 000 L dose of TMA due to the deposition of methyl groups. The blue bars in Fig. 6 show a final dose of atomic H results in reduction of carbon signal due to desorption of methane and/or removal or additional surface carbon and the oxygen signal remains just above the detection limit of the XPS.

The raw XPS spectra, Figs. S2-S5, show a shift toward lower binding energy after the initial H clean due to removal of oxide. The non-wet cleaned samples, Figs. S3 and S5, have much larger C and O signals and the InGaAs is also oxidized indicated from higher binding energy peaks. After the TMA dose, the C signal increases due to methyl deposition and the C signal is reduced after final H clean.³³ This study emphasizes the need for an *in situ* dry surface cleaning method. The *ex situ* BOE did not have the same cleaning effects on both the (001) and (110) surfaces while the atomic H had a very similar cleaning effect on both surfaces. In fabricating a 3D device, it is crucial to simultaneously clean all faces of the devices to ensure pristine surfaces prior to further processing.

The D_{it} energy profiles of several of the samples from Figs. 1-5 were extracted using the full interface state model, Fig. 7.¹⁹ The full interface state model uses a Y circuit which introduces additional capacitance proportional to D_{it} at the Fermi energy. A rigorous treatment, which converts the Y circuit to a Δ circuit for the integration with respect to trap energy, is then applied to calculate the total multi-frequency capacitance and conductance. By matching the calculated capacitance and conductance with the experimental result, D_{it} as



FIG. 6. XPS ratios of the same process matrix as in the previous two figures are presented. The carbon and oxygen signals are normalized to the sum of the substrate peaks. For the (001) samples (top row) the amount of C and O is reduced when receiving a BOE for the asloaded samples (red). The (110) sample (bottom row) shows a reduction in C but no change in the amount of O for the as-loaded samples (red). This suggests the (110) surface is less prone to oxidation and explains the similar CV curves observed in Fig. 4. After exposing the surfaces to atomic H (green) the amount of C and O is reduced to similar levels for the (001) and (110) samples. This demonstrates the effectiveness of a dry etch compared to the wet clean on both surfaces. A dose of TMA (purple) results in a small increase in C signal due to the presence of methyl groups. A final dose of atomic H reduces the C signal from methane desorption.

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FIG. 7. D_{it} extracted using the full interface state model. The sample which was exposed to H plasma only at 300 °C (red square) exhibits a much higher D_{it} than any of the other samples which is a result of plasma induced damage. The sample exposed to H plasma at 120 °C (purple x) shows a slightly higher D_{it} in the upper half of the bandgap compared to the other samples. This again is attributed to plasma damage. The samples exposed to H/TMA/H at 120 °C and 300 °C (green triangles, blue diamond) exhibit the lowest D_{it} of the samples modeled. All samples which had TMA incorporated into the pandgap regardless of temperature or *ex situ* wet cleans. This emphasizes the importance of TMA in the *in situ* clean to allow for pristine surfaces regardless of crystal face.

a function of surface energy can be extracted. This method proves to extract D_{it} reliably and consistently in high-k/InGaAs MOS capacitors.^{15,36} The sample which was exposed to 10 cycles of H plasma at 300 °C (red square) exhibits a dramatically higher D_{it} than any of the other samples, which was

suggested by the magnitude of the false inversion bump. The sample that was exposed to atomic H at 120 °C (purple x) exhibits a slightly higher D_{it} than any of the other samples in the upper half of the bandgap. All samples which had TMA incorporated into the pre-ALD clean, regardless of the process temperature or ex situ BOE cleaning, exhibit very similar D_{it} values of $2 - 3.8 \times 10^{12}$ cm⁻² eV⁻¹ at $E - E_c = -0.5$, Table I. The samples do show a greater variation in the D_{it} toward the VB. However, in an n-channel flat band architecture III-V MOSFET, the Fermi level is only modulated in the upper half of the bandgap making interface states below the mid gap less significant for limiting device performance. A method for extracting the border trap densities (Nbt) was developed by Taur et al. which assumes a spatially uniform N_{bt} distribution in the oxide and takes into account the influence of Cmax on frequency dispersion in accumulation. The densities are extracted by matching the frequency dispersion at the accumulation regions of both the CV and conductance-voltage (GV) curves.³⁶

The border trap densities (N_{bt}) were also extracted, Table I. All samples which had TMA incorporated into the pre-ALD surface clean had N_{bt} values between 1.7 and 2.4 $\times 10^{20}$ cm⁻³ eV⁻¹. The sample which was exposed to H only at 300 °C had a N_{bt} of 3.0×10^{20} cm⁻³ eV⁻¹. The majority of samples processed at 120 °C had a lower D_{it} than the samples processed at 300 °C and statistical analysis showed, using an alpha value of 0.05, a p value of <0.05 indicating lowering the ALD temperature resulted in reduction of D_{it}. An α value of 0.05 indicates the results having 95% chance of being a direct result of manipulation of experimental variables, while obtaining a p value less than the α value, (<0.05), suggests that these results are due to the temperature differences.

TABLE I. Peak D_{it} and N_{bt} densities. Samples which received H/TMA/H treatment have N_{bt} densities between 1.9 and 2.2×10^{20} cm⁻³ eV⁻¹. The sample which received exposure to H plasma only at 300 °C exhibits a much higher density of border traps. This indicates that TMA reduces the number of trap states at the InGaAs/HfO₂ interface and minimizes defects in the oxide. All samples which had TMA incorporated into the pre-ALD clean have D_{it} values between 2.0 and 3.8×10^{12} cm⁻² eV⁻¹, whereas the samples exposed to H alone at 120 °C has 3.8×10^{12} cm⁻² eV⁻¹ and the sample exposed to H alone at 300 °C has 14×10^{12} cm⁻² eV⁻¹. Thus, TMA plays an important role in minimizing both interface defects and border traps regardless of crystal face, temperature, or *ex situ* wet cleans. It is noted that the 120 °C sample consistently had a lower D_{it} than the 300 °C sample; a statistical analysis was performed which showed this difference had a p value of <0.05.

	V _{th} (V)	C_{ox} (μ F/cm ²)	N_{bt} (×10 ²⁰ cm ⁻³ eV ⁻¹) @ E - E _c = 0.5 V	D_{it} (×10 ¹² cm ⁻² eV ⁻¹) @ E-E _c = 0.5 V
	. 10 ()	-0, (/ •)		
(001) 10 cycles H only 120 °C/300 °C	0.63/0.53	4.3/5.3	2.2/3.0	3.8/14
(001) 2 cycles H/TMA 120 °C/300 °C	0.57/0.50	4.8/6.5	1.8/2.0	3.8/3.5
(001) 5 cycles H/TMA 120 °C/300 °C	0.55/0.50	4.5/4.9	1.7/1.9	2.7/3.3
(001) 10 cycles H/TMA 120 °C/300 °C	0.60/0.62	3.7/5.5	1.9/2.2	2.0/2.0
(001) BOE 120 °C/300 °C	0.57/0.63	3.8/4.8	2.3/2.1	2.9/3.4
(001) no BOE 120 °C/300 °C	0.56/0.60	5.2/6.8	2.4/2.0	2.8/3.4
(110) BOE 120 °C/300 °C	0.59/0.50	4.5/6.0	2.2/1.9	2.8/3.2
(110) no BOE 120 °C/300 °C	0.59/0.55	4.6/5.5	2.1/2.0	2.8/3.5

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This indicates that TMA-based surface treatment not only reduces the density of defects at the InGaAs/HfO2 interface but also results in a more robust oxide, as border traps are associated with defects within the oxide and are thought to be located within about 1 nm from the semiconductor/oxide interface.³⁷ The oxide capacitances (Cox) at 120 °C and 300 °C vary due to anomalies in the ALD growth rate which can qualitatively influence the apparent magnitude of D_{it} bump but the quantitative D_{it} will not be influenced since C_{ox} is factored in when extracting the Dit. While it is possible that, under some processing conditions, thinner oxide may have higher D_{it} due to defect generation in metallization, it has been reported that D_{it} can be nearly invariant with oxide thickness.³⁸

Even though the lowest D_{it} values reported in this study are 1-2 orders of magnitude greater than those typical of SiO₂/Si interfaces, the obtained values are low for high-k/InGaAs gate stacks, which typically display Dit values in the range of 1.0 $\times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ to $1.0 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$.^{16,39,40} In addition, there are several potential pitfalls in Dit analysis of III-V MOS devices, requiring application of methods, such as the full interface state model used in this report, that avoid unphysical D_{it} extraction and underestimation of the trap density¹⁹ that may affect other results described in the literature. Finally, the interface defects densities observed for the studied HfO₂/InGaAs gate stacks are well within the useful range for potential application in end-of-roadmap MOS devices. Due to the very high Cox values (low EOT) that would pertain for such devices, the effect of Dit on flat band voltage shift and subthreshold swing is greatly reduced,⁴¹ making HfO₂/InGaAs a strong candidate for future MOS transistors.

CONCLUSION

In situ STM and XPS were employed to determine the role of TMA in a pre-ALD surface clean developed by Carter et al. and Chobpattana et al. and to determine the effectiveness of this clean on the InGaAs (110) surface. By employing STM, XPS, and CV profiling, TMA was determined to prevent and clean up etch damage caused by the atomic H. Consistent with the reduction of H induced etch damage, incorporating TMA reduced the magnitude of interface trap states at both 300 °C and 120 °C by minimizing and preventing the formation of In/Ga clusters. Lowering the temperature alone resulted in reduction of trap states, but not to the same extent as when including TMA. An ex situ BOE was examined on both the In-GaAs (001) and (110) surfaces. The BOE efficiently removed both carbon and oxygen on the (001) surface but only removed carbon on the (110) surface. This emphasizes the need for an all dry pre-ALD surface clean when depositing material on 3D structures since this will allow for efficient nucleation of ALD precursors on all crystal planes.

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