Cleaning and Passivation of the Four Horseman of the Silicon Apocalypse

T. J. Kent[1], M. Edmonds[1], M. Chang[3], J.Kachian[3], R. Droopad[4], E. Chagarov[2], and A. C. Kummel[1,2]
[1]Materials Science and Engineering Department, University of California San Diego
[2]Department of Chemistry and Biochemistry, University of California San Diego
[3]Applied Materials, Sunnyvale, California
[4]Ingram School of Engineering, Texas State University

INTRODUCTION

In-situ atomic imaging of cleaning and passivation of several systems has been studied. (1) For InGaAs (001), a low temperature in-situ cleaning process has been combined with low temperature HfO_2 ALD to reduce the EOT below 0.4 nm. (2) For InGaAs (110), STM/STS studies have shown that both a metal precursor (TMA) and an oxidant (H_2O) are required to remove trap states. (3) To assist in utilizing similar gate and contact processing on group IV and InGaAs surfaces, a silicon monolayer ALD process has been developed for InGaAs (001). (4) SiGe combines the most challenging components of cleaning Si and Ge; using a reaction with HOOH (g) and post deposition annealing, SiGe (001) becomes terminated with Si-OH which is nearly ideal for ALD nucleation.

RESULTS

A limiting factor in the transition to using III-V channels with high-k dielectrics in MOSFETs is the large density of interfacial trap states (D_{it}) at the semiconductor/oxide interface[1]. These trap states result from undercoordinated atoms at the interface, metallic bonds, strained bonds, and intermixing[2]. All of these can result from poor nucleation of the atomic layer deposition (ALD) high-k precursors.

DFT simulations were performed with the Vienna Ab-Initio Simulation Package (VASP) using projector augmented-wave (PAW) pseudopotentials (PP) and the PBE (Perdew-Burke-Ernzerhof) exchange-correlation functional. The choice of PBE functional and PAW PP was validated by parameterization runs demonstrating good reproducibility of experimental lattice constants, bulk moduli, and formation/cohesive energies for bulk crystalline GaAs. DFT calculations show that a high nucleation density allows for an unpinned interface even with direct bonding between the high-k and $In_{0.5}Ga_{0.5}As(001)$ (see Fig. 1)[3]. However, several types of oxide/InGaAs imperfections which can induce midgap state formation and Fermi level pinning were identified. (a) Conduction band edge states are usually formed by the metallic group III-group III bonds (In-Ga, Ga-Ga, In-In) present at defect sites even on the

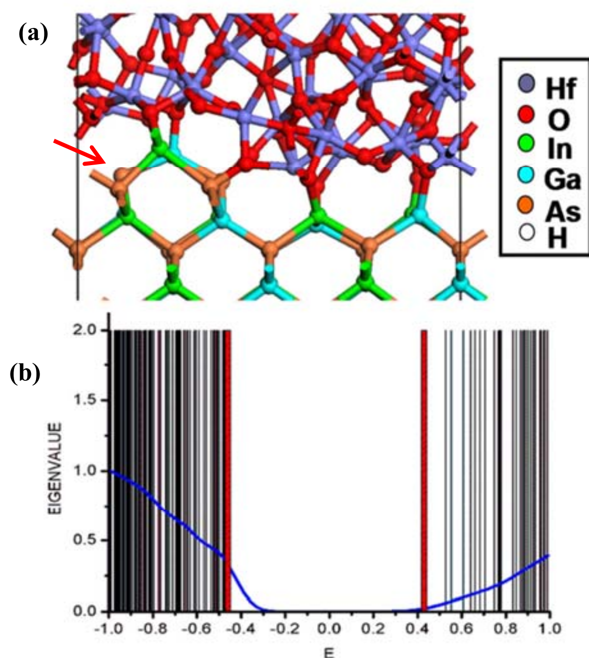

FIGURE 1: DFT Model of Fully Bonded a-HfO_2/InGaAs Interface; (a) Interface structure of a-HfO_2/InGaAs (001) after annealing at high temperature. For the model, there is only one dangling bond which is a filled dangling bond on an As atom (red arrow). (b) DOS and eigenstates for annealed a-HfO_2/InGaAs. The band gap of the clean surface is shown by the red lines. The lack of band gap states shows that direct bonding of high-k dielectric can form an unpinned interface as long as the surface is not disrupted and there are no partially filled dangling bonds[3].

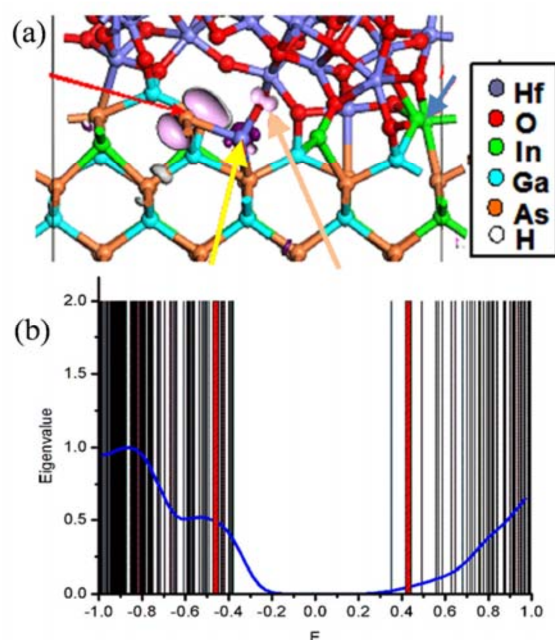

FIGURE 2: DFT Model of an underbonded a-HfO_2/InGaAs Interface With Intermixing: (a) Interface structure of a-HfO_2/InGaAs(001) after annealing at high temperature. Note one Hf atom (yellow arrow) has migrated from the HfO_2 to the InGaAs (b) DOS and eigenstates for annealed intermixed a-HfO_2/InGaAs. The band gap of the clean surface is shown by the red lines. The major valence band edge state (pink) is on the As (red arrow) which lost its bond to In atom (blue arrow) and formed a new bond to the intermixed Hf atom (yellow arrow). The major CB states are on the Hf atom (yellow arrow) which diffused into the InGaAs; this Hf also has associated VB states on itself and on a nearby O atom (brown arrow) [3].

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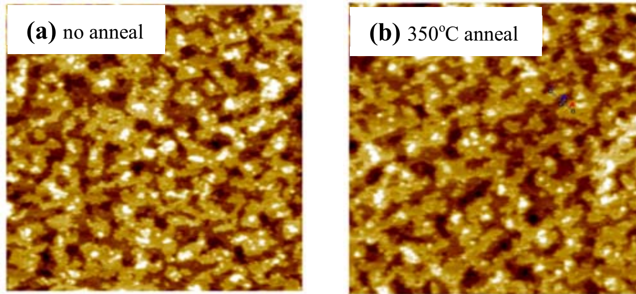

FIGURE 3: Effect of PDA on Atomic H Cleaning of InGaAs(110);100 nm x 100 nm images. (a) InGaAs (110) was exposed to thermal atomic H at 275 ˚C. The islands have single steps which are 0.24 nm tall. The white sites are remnants of etching of the top layer. (b) Post-Deposition Annealing (PDA) at 350 ˚C for 30 minutes slightly reduced the white sites but the high step density remains.

clean surface, and at InGaAs surface atoms with semiconductor bonds broken during bonding to the oxide (b). If there is intermixing between the oxide and InGaAs, both conduction and valance band edge state will form [3]. An example is shown in Fig 2. In this example, a Hf atom has migrated from the oxide to the InGaAs surface inducing formation of CB states on undercoordinated As atoms and a VB state on the Hf. However, uncoordinated As atoms with filled dangling bonds do not include states in the band gap (Fig 1). Having an unpinned interface after full oxide/semiconductor bonding is all predicated on the InGaAs being clean (free of C and O) prior to oxide deposition.

Subcutaneous oxidation and plasma damage during in-situ cleans can also generate trap states at the interface. Melitz et al. and Kent et. al. [4-5] showed it is possible to use atomic H to remove oxide from InGaAs surfaces while Carter et al.[6] showed that exposing the InGaAs surface to a pulse of H_2 plasma followed by a pulse of TMA can reduce the D_{it} in a device fabricated with Al_2O_3 as the gate oxide. Chobpattana et al.[7] demonstrated that adding a second pulse of H_2 plasma, post TMA pulse, can improve device performance when depositing HfO_2 at 300 ˚C. In the present study, HfO_2 ALD was performed at 120 ˚C to limit the diffusion of H_2O and O_2, which have been shown to diffuse readily through HfO_2 and to minimizing plasma damage[8]. The effectiveness of an ex-situ buffered oxide etch (BOE) was determined as well as an in-situ H plasma/TMA/H plasma pre-ALD clean. The 120 ˚C results were compared to the same set of experiments performed at 300 ˚C to determine the effect of temperature on the nucleation of HfO_2. HfO_2 ALD at 120 ˚C resulted in significantly reduced plasma damage during the pre-ALD clean. By incorporating a pulse of TMA the damage was minimized at both 120 ˚C and 300 ˚C. The BOE was effective on the (001) surface but had no effect on the (110) surface necessitating the need for an in-situ dry clean to maximize nucleation on both crystal faces simultaneously.

Hydrogen cleaning of InGaAs (110) is quite challenging since it can result in etching and the formation of a rough interface which is not removed by annealing[5] (Fig 3); however, the combination of atomic H cleaning and TMA results in a low interface roughness since the TMA acts as a vapor deposited etch stop for atomic H. While this is most critical on InGaAs (110), even low dose atomic hydrogen cleaning of InGaAs (001) leaves increased step density after a long high temperature anneal (Fig 4).

A broader range of channel materials allowing better carrier confinement and mobility could be employed if a universal control monolayer (UCM) could be ALD or self-limiting CVD deposited on multiple materials and crystallographic faces. This study focuses on depositing a saturated Si-H seed layer via two separate self-limiting and saturating CVD processes on InGaAs (001)-(2x4), and SiGe(001). XPS, STS/STM, and DFT simulations were employed to characterize the electrical and surface properties of the saturated silicon seed layers on InGaAs (001)-(2x4). STM shows the self-limiting CVD process results in a commensurate structure with average row spacing at 1.5-1.6 nm, consistent with III-V dangling bond elimination. DFT simulations show InGaAs surface passivation with $Si\text{-}H_x$ is achieved with satisfaction of the electron counting rule and an unpinned surface Fermi level.

For SiGe (001) and SiGe (110), the main challenge is to avoid formation of GeO_x. This can be accomplished by either forming a Si terminated surface via functionalization to an oxygen containing ligand or by deposition of a silicon monolayer. The SiGe (110) surface has the additional challenge that the clean surface is terminated by a monolayer of atoms with half-filled dangling bonds so every atom must be functionalized to remove the Fermi level pinning.

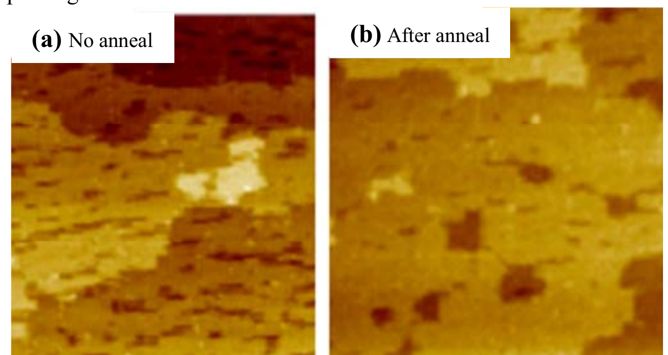

FIGURE 4: Effect of PDA on Atomic H Cleaning of InGaAs(001)-(2x4);100 nm x 100 nm images. (a) Air exposed InGaAs (001) was dosed with atomic H at 380˚C. Note the high density of small etch pits. (b) Post Deposition annealing (PDA) at 480˚C restores (2x4) reconstruction and lowered edge pit density

SUMMARY

Among the requirements to forming an unpinned interface on InGaAs (001), InGaAs (110), SiGe (001), and SiGe (110) are (a) removal of carbon and oxygen prior to oxide deposition, (b) abrupt bonding of the oxide to the surface without intermixing, and (c) elimination of half-filled dangling bonds. The in-situ cleaning process is critical but even the most gentle method (cleaning with atomic H) can induce formation of steps and dangling bonds. To ensure elimination of the half-filled dangling bonds requires functionalization of every surface atom.

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