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Sub-Nanometer Interfacial Oxides on Highly Oriented Pyrolytic Graphite and Carbon Nanotubes Enabled by Lateral Oxide Growth

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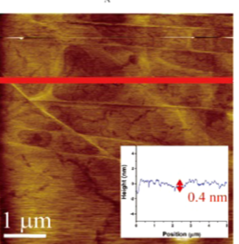
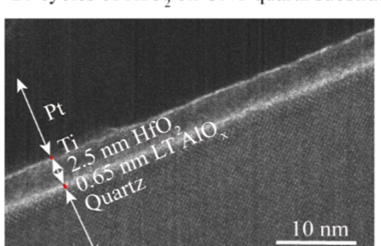
ABSTRACT: A new generation of compact and high-speed electronic devices, based on carbon, would be enabled through the development of robust gate oxides with sub-nanometer effective oxide thickness (EOT) on carbon nanotubes or graphene nanoribbons. However, to date, the lack of dangling bonds on sp^2 oriented graphene sheets has limited the high precursor nucleation density enabling atomic layer deposition of sub-1 nm EOT gate oxides. It is shown here that by deploying a low-temperature AlO_x (LT AlO_x) process, involving atomic layer deposition (ALD) of Al_2O_3 at 50 °C with a chemical vapor deposition (CVD) component, a high nucleation density layer can be formed, which templates the growth of a high-*k* dielectric, such as HfO_2. Atomic force microscopy (AFM) imaging shows that at 50 °C, the Al_2O_3 spontaneously forms a pinhole-free, sub-2 nm layer on graphene. Density functional theory (DFT) based simulations indicate that the spreading out of AlO_x clusters on the carbon surface enables conformal oxide deposition. Device applications of the LT AlO_x deposition scheme were investigated through electrical measurements on metal oxide semiconductor capacitors (MOSCAPs) with Al_2O_3/HfO_2 bilayer gate oxides using both standard Ti/Pt metal gates as well as TiN/Ti/Pd gettering gates. In this study, LT AlO_x was used to nucleate HfO_2 and it was shown that bilayer gate oxide stacks of 2.85 and 3.15 nm were able to achieve continuous coverage on carbon nanotubes (CNTs). The robustness of the bilayer was tested through deployment in a CNT-based field-effect transistor (FET) configuration with a gate leakage of less than 10^{-8} A/μm per CNT.

AFM of 10 cycles LT AlO_x on HOPG



TEM of 6 cycles of LT AlO_x and 20 cycles of HfO_2 on CNT quartz substrate



KEYWORDS: *effective oxide thickness, atomic layer deposition, carbon nanotubes, field effect transistor, metal oxide semiconductor capacitors*

1. INTRODUCTION

New materials and related technologies are necessary to promote and enable scaling of electronic devices to the atomic scale.[1] Use of Si and SiGe FinFETs may be challenging at these dimensions due to their low carrier mobility (<100 cm^2/V s) and difficulties in strain engineering in nanowire geometries.[2,3] However, carbon nanotubes (CNTs) have higher mobility, exceeding 3000 cm^2/V-s,[4,5] and are less susceptible than Si/SiGe FinFETs to short-channel effects due to the ∼1 nm body thickness. The increased mobility enables drive currents in excess 10 μA/CNT, while the band gap (∼0.8 eV/d_t, where d_t is the CNT diameter) enables an on/off switching ratio exceeding five orders of magnitude.[6] There have also been reports of sub-threshold swings possibly less than 59 mV/decade, from tunneling assisted processes in CNT-based devices.[2,5,7−11]

A major problem in the fabrication of single CNT-based field-effect transistors (FETs) has been the growth of a high dielectric constant (high-*k*) gate oxide on CNT channels. The on/off ratio and sub-threshold slope should be preserved even as the gate length is reduced to 10 nm provided that there is a robust, low leakage, low effective oxide thickness (EOT) dielectric. However, the chemically passive nature of CNT surfaces poses a challenge for deposition of low defect density, sub-1 nm EOT gate oxides through the use of traditional methodologies, *e.g.*, atomic layer deposition (ALD). Generally, for chemically inert surfaces, ALD preferentially occurs on defect sites or grain boundaries,[12−22] which are absent in CNTs. Although many different surface preparation methods have been studied and reported for ALD on highly oriented

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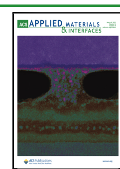

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pyrolytic graphite (HOPG)[1,14,23−25] including the use of polymer seeding layers,[23,24,26−29] ozone,[16,22] NO_2,[30] and plasma[16,21,31] treatments, such methods increase the EOT of the gate stack or decrease the mobility of the semiconducting channel by introducing defects or charge trapping sites.[32] A direct deposition of the gate oxide is preferable and is shown to be feasible in this work.

In the present report, it is shown that ALD may be optimized for high quality and conformal gate oxide deposition with precise control of the layer thickness on CNTs. It was previously reported that aluminum oxide (Al_2O_3) could be deposited conformally on top of HOPG surfaces by a low-temperature ALD process without any seeding layers and surface pretreatment.[6,33] The related principles for producing a pinhole-free, sub-2 nm Al_2O_3 film are first extended on HOPG to investigate the film nucleation mechanism during the first several deposition cycles. By tuning the precursor pulse, purge time, and the substrate temperature, sub-nanometer low-temperature AlO_x (LT AlO_x) particles are formed which nucleate on the HOPG surface. By increasing the number of deposition cycles while recording the film coverage by atomic force microscopy (AFM), the spread of LT AlO_x across the HOPG surface was observed. This is unexpected since weak absorbate−substrate interactions normally induce island growth instead of conformal growth. To further verify the film growth mechanism, DFT simulation was performed which showed that the lateral growth of LT AlO_x was energy favorable during the first several deposition cycles. For proof of principle that practical devices could be constructed from the deposited oxides, Al_2O_3 was used as a template for subsequent high-k gate oxide (*e.g.*, HfO_2) deposition. For the determination of the dielectric constants, the capacitance of Al_2O_3/HfO_2 bilayer-based gate oxides, on both HOPG and Si, were investigated. A high capacitance together with the related dielectric constant was taken as a measure of the bilayer quality. Gettering gates have been shown to reduce the interfacial oxide thickness[34] and were also deployed for further EOT scaling. The high bilayer performance, *e.g.*, with respect to low gate leakage current, and low sub-threshold swing were confirmed on CNT-based FETs through current (I)−voltage (V) measurements. X-ray photoelectron spectroscopy (XPS) was performed for the analysis of the chemical composition of LT AlO_x and the result indicated that such a film was oxygen-rich compared to high-temperature Al_2O_3.

2. EXPERIMENTAL SECTION

2.1. ALD of Al_2O_3 and HfO_2. LT AlO_x-related ALD was performed on both 1 mm thick, grade 1 HOPG (SPI Inc.), and Si(100) substrates (University Wafers, Inc.). The HOPG substrates were mechanically exfoliated using Scotch tape to form a pristine surface. The Si wafers were cleaned by sequential dips in acetone, isopropyl alcohol, and deionized (DI) water for 30 s each. The native oxide was removed from the Si samples using a cyclic HF clean consisting of sequential dips in 2% HF solution and DI water at room temperature for 1 min in each solution for a total of 2.5 cycles ending in HF. The HOPG and Si samples were transferred into an ALD reactor (Beneq TFS 200). Trimethylaluminium (TMA) and water (H_2O) were used as precursors with N_2 purge gas with deposition temperatures between 50 and 70 °C. Two to ten cycles of ALD were performed for nucleation studies on HOPG. Each ALD cycle consisted of the following four steps: (i) a TMA pulse, (ii) a N_2 purge, (iii) a H_2O pulse, and (iv) a N_2 purge. The pulse and purge times were varied. Typically, a 750 ms TMA, 3 s N_2 purge time, 850 ms H_2O, and 3 s N_2 purge times were used. This ALD process with chemical vapor deposition (CVD) component had a growth rate of about 1.4 Å/cycle on the Si substrate measured by ellipsometry. The low-temperature ALD process is tool dependent, but it has been reproduced using a different tool by Lin et al.[35] When the process is transferred to a new tool, the key parameters to be adjusted are the pulse lengths and purge times while the temperature can remain constant.

For the bilayer samples, on top of a LT AlO_x templating layer (10 cycles of ALD), HfO_2 of different thicknesses (corresponding to 40−90 cycles of ALD) were deposited at 200 °C. Tetrakis-(dimethylamido)hafnium(IV) (TDMAH) and H_2O were used for high-k dielectric precursors, and the HfO_2 was deposited in another ALD reactor (Cambridge Nanotechnology, Fiji) at 200 °C. A cycle consisted of a sequence of the following four steps: (i) a H_2O pulse, (ii) a N_2 purge, (iii) a TDMAH pulse, and (iv) a N_2 purge with 60 ms H_2O and 250 ms TDMAH pulse time and a 15 s N_2 purge time. The growth rate of HfO_2 was about 1.0 Å/cycle on the Si substrate measured by ellipsometry. The bilayer (10 cycles of LT AlO_x and 20 cycles of HfO_2) was also deposited on top of aligned CVD-synthesized single-walled CNTs on ST-cut quartz substrates, but for these CNT samples, a gettering gate was employed to further scale the gate stack EOT.

2.2. Atomic Force Microscopy (AFM), Spectroscopic Ellipsometry, and Transmission Electron Microscopy (TEM). The morphology of the deposited LT AlO_x on HOPG substrates was studied by atomic force microscopy (AFM) (Agilent Technologies 5500). For deposition on Si(100), spectroscopic ellipsometry (JA Woollam M 2000) was used to measure the thickness of the deposited oxide. The deposition rate was determined to be on the order of 0.14 nm per cycle over the tested range of cycles on Si(100). The cross-sections for the films deposited on HOPG were studied by transmission electron microscopy (TEM).

2.3. Capacitor and FET Test Structures. For capacitor fabrication, the bottom electrode was the HOPG or Si substrate while sputter deposition (Denton 18, 200 W, 5 mTorr) was employed for the fabrication of the top electrodes. Additionally, gettering gate stacks with TiN (6 nm)/Ti (7 nm)/Pd (6 nm) were sputter-deposited on samples with bilayer oxides. The top electrode had a contact diameter of 150 and 60 μm for the Si and HOPG substrates, respectively. To avoid any slip during the top gate deposition, a shadow mask and the Si and HOPG substrates were compressed tightly by a glass slide. All top gates were checked using a microscope.

For gate leakage study, top-gated CNTFET was prepared and the detailed process flow is shown in Section 1 of the Supporting Information. LT AlO_x was first deposited on pristine CVD-grown CNTs. Then the active region was defined by photolithography. A 2% tetramethylammonium hydroxide (TMAH) solution (MF-26A) was used to remove and pattern LT AlO_x, while oxygen plasma was used for removing the CNTs. The source and drain contacts were patterned by photolithography, followed by Ti (1 nm)/Pt (20 nm) films and a standard lift-off process. HfO_2 was deposited by ALD. Subsequently, vias for electrical probing were patterned by photolithography. Finally, the gate was patterned by photolithography, followed by electron-beam evaporation (EBE) deposition of a Ti (1 nm)/Pt (20 nm) film and a standard lift-off process. A second version of the device process used the sputtered TiN (22.8 nm)/Ti (10.7 nm)/Pd (87.2 nm) gate metal. The use of a gettering gate enhanced the k values for both LT AlO_x and HfO_2 dielectric layers.

For transistor performance study, short-channel CNTFET was prepared and the detailed process flow is shown in Section 2 of the Supporting Information. A TiN (10 nm) film was deposited by sputter deposition followed by Al_2O_3 (7.5 nm) through ALD. Aligned CNTs were then transferred on top of the Al_2O_3 layer. The source and drain regions were defined by electron-beam lithography (EBL), followed by evaporating a Pd (10 nm) film and a standard lift-off process. Subsequently, an active region was patterned *via* EBL followed by O_2 plasma (Oxford Plasma 80). Twenty cycles of LT AlO_x and 20 cycles of HfO_2 were deposited. EBL was used again for pattering vias, which were used for electrical probing. A buffered oxide etchant (6:1) was used to remove the AlO_x and HfO_2. Finally, the top

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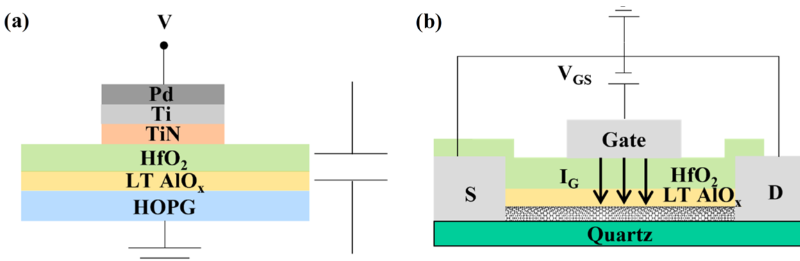

Figure 1. Electrical characterization geometry for LT AlO_x and high-*k* dielectric (HfO_2) bilayer gate oxides. (a) Schematic for the MOSCAP measurement using a gettering gate stack (TiN/Ti/Pd). (b) Schematic for the CNTFET measurement. For CNTFETs, Ti/Pt and gettering gate metals were employed. For the CNTs, a bilayer physical thickness of ~3.15 nm was observed by TEM with an LT AlO_x layer of only 0.6 nm.

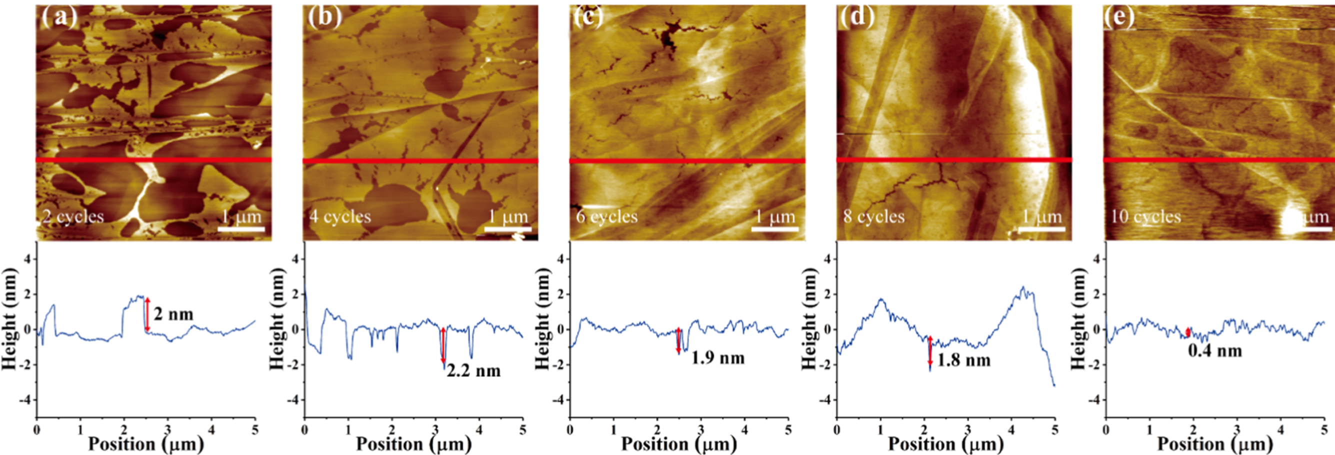

Figure 2. AFM images and analysis of variable cycles of LT AlO_x on HOPG. (a−e) 2, 4, 6, 8, and 10 deposition cycles at 50 °C. Below each image is a line trace corresponding to the red line in the AFM images. The depths of the lakes and cracks were used to determine the film thickness. Note the data are consistent with the film filling the voids by spreading laterally across the surface.

gate was patterned through EBL followed by Pd (30 nm) deposition through EBE.

2.4. Electrical Characterization. The capacitance−voltage (*C*−*V*) and current−voltage (*I*−*V*) characteristics of the capacitors were probed using a Keithley 4200A SCS parameter analyzer. *C*−*V* was investigated in a frequency range from 5 kHz to 1 MHz. *C*−*V* was scanned from +2 to −2 V with a step size of 0.05 V. Leakage current density was also recorded. The gate leakage and transfer characteristics of CNTFETs were measured in the range of −5 to +5 V (Keysight B1500) with a step size of 0.01 V.

2.5. XPS Spectra. The X-ray photoelectron spectroscopy (XPS) was performed *ex situ* using a UHV analysis (Omicron VT, base pressure 5×10^{-10} Torr) chamber. High-resolution XP spectra were acquired using a Mg Kα source ($h\nu$ = 1253.6 eV) and DESA 150 electron analyzer (Staib Instruments) at a collection angle of 45° relative to the surface normal using a step width of 0.1 eV. Analysis of the XPS data was performed using CasaXPS v2.3 with Shirley background subtraction and Scofield photoionization cross-section relative sensitive factors. The core spectra were calibrated with a carbon correction of 284.8 eV.[36] Samples were approximately 15 nm thick and underwent no surface preparation (*e.g.*, Ar-ion sputtering or UHV annealing) prior to data collection.

3. RESULTS AND DISCUSSION

To validate the quality of the deposited LT AlO_x/HfO_2 bilayer oxide films, electrical characterization was carried out as indicated in Figure 1. A HOPG metal oxide semiconductor capacitor (MOSCAP) is shown in Figure 1**a**, while a FET-based measurement configuration using CNTs on a quartz substrate is illustrated in Figure 1**b**.

It was previously reported that the LT AlO_x film morphology on HOPG was highly sensitive to the substrate temperature.[37] At T_{sub} > 100 °C, the deposition was predominantly along the step edges while at lower temperatures (<80 °C), the LT AlO_x film was nucleated in the terrace regions. It was earlier hypothesized that the TMA and H_2O precursors react in the gas distribution unit (GDU) of the ALD system to form reactive species (such as sub-1 nm AlO_xH_y particles) prior to impinging on the surface due to the short purge time. However, no surface imaging was performed to confirm the mechanism or to document the deposited film roughness. An understanding of such aspects is critical to determine the extent to which the thickness may be scaled on channels of different sizes and materials.

3.1. AFM Morphology and Analysis. For clarifying the nucleation and growth mechanisms related to LT AlO_x, a HOPG substrate was exposed to 2−10 cycles of ALD with an optimal, fixed purge time at three different substrate temperatures, *i.e.*, 50, 60, and 70 °C. The reaction conditions were 750 ms TMA, 3 s N_2 purge time, 850 ms H_2O, and a 3 s N_2 purge time. AFM images of the surface are shown in Figure 2. With 2 deposition cycles (Figure 2**a**), the LT AlO_x deposition was initiated along step edges with some coverage on the terrace regions. The AFM line trace measurements were used to determine the film thickness and are shown below the images. Note, even though the deposition may have initiated at the step edges, the final Al_2O_3 layers were relatively smooth with a thickness of ~2 nm. With 4 cycles of LT AlO_x (Figure 2**b**), the step edges were covered, and the film growth

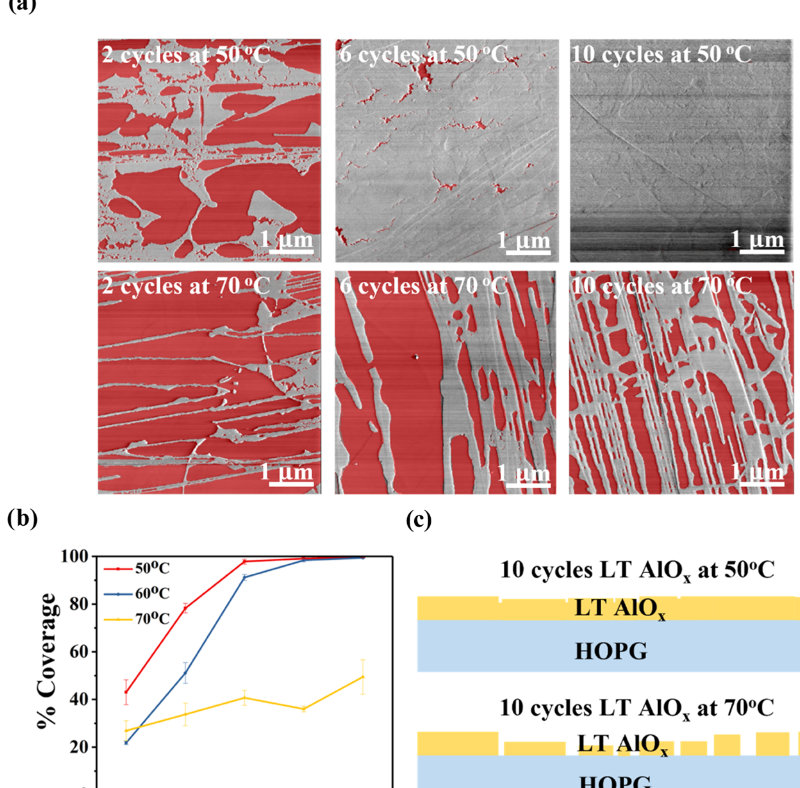

Figure 3. Image analysis of AFM micrographs of LT AlO_x coverage on HOPG as a function of temperature. (a) Image analysis of 2, 6, and 10 deposition cycles at 50 and 70 °C. The red lake region is the uncovered HOPG surface while the gray plateau region is LT AlO_x. (b) Percentage coverage *vs* number of cycles of Al_2O_3 LT AlO_x at 3 temperatures. (c) Schematics of LT AlO_x coverage with 10 deposition cycles at 50 and 70 °C.

increased on the terrace regions while maintaining 2 nm thickness. The uncovered regions of the terraces appeared as dark "lakes" in AFM. With 6 cycles of LT AlO_x (Figure 2c), the majority of the lakes disappeared, but pinholes and worm-like cracks were still present, and the thickness as measured *via* the cracks was still ∼2 nm. With a further increase in the deposition cycles (8 cycles in Figure 2**d** and 10 cycles in Figure 2**e**), the pinholes disappeared, with a related reduction in the number of cracks. The line traces were consistent with a uniform LT AlO_x film thickness (∼2 ± 0.2 nm) for 2−8 cycles. The thickness of the LT AlO_x layer as determined by AFM was verified in the full stack structure using TEM. The TEM study in Figure 5**d** showed that LT AlO_x quantified as 2 nm by AFM was only 1.34 nm when quantified by TEM. The sub-nanometer reduction in film thickness may be due to scavenging of oxygen by the Hf precursor,[38] slight intermixing with the HfO_2, or the limitations of the AFM technique. All TEM measurements require the deposition of a capping layer so TEM of the LT AlO_x without HfO_2 was not attempted. Therefore, the absolute thickness as measured by AFM is considered to be an upper limit, but the relative thicknesses as measured by AFM are considered to be accurate. The filling of the cracks with increasing LT AlO_x deposition was observed by comparing Figure 2**d**,**e**, where the measured depth was reduced from 2 to ∼1.8 nm and further to ∼0.4 nm.

AFM analysis was also performed after LT AlO_x deposition on HOPG at a higher substrate temperature, (60 and 70 °C) as shown in Figures S3 and S4. Similar to what was observed at 50 °C, (Figure 2**a**−**e**), an increasing number of LT AlO_x deposition cycles resulted in lateral growth of a constant thickness film spreading from the step edges over the terraces.

Quantitative analysis of the coverage as a function of substrate temperature over a 5 μm × 5 μm area (using Gwyddion image analysis software) is shown in Figure 3**a** and analyzed in Figure 3**b**. As expected, the coverage increased with the number of deposition cycles, but additional aspects of the growth mechanism are indicated, as follows: (1) at lower temperature (50 °C), with 10 deposition cycles, the coverage was close to complete while only ∼50% coverage was achieved at a higher temperature (70 °C). (2) At 50 and 60 °C, the greatest increase in coverage occurred over the first six cycles (Figure 3**b**). The corresponding schematic for the growth of LT AlO_x is shown in Figure 3**c**. To understand the uncovered region size distribution, a detailed percentage of total open area distribution for each temperature is depicted in Figure S5. Detailed analysis of the total open area showed that at low cycles, the presence of large (>10^5 nm^2) lakes accounted for the majority of the open area, regardless of temperature. At low temperatures and slightly higher cycles, the major contribution to the uncovered regions became small (<10^3 nm^2) size lakes or medium (10^3−10^5 nm^2) size lakes (at 50, 60 °C, respectively). While at 70 °C, large (>10^5 nm^2) size lakes remained the primary contributor to the total weighted open areas.

The observations from the AFM imaging are consistent with the hypothesis that TMA and H_2O react with each other in the GDU forming AlO_x clusters (LT AlO_x), which are subsequently deposited on the surface.[37] The initial LT AlO_x

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nucleation on HOPG at the step edges and related defects is due to the dangling bonds in these regions forming reactive sites with high surface free energy. However, on low defect substrates such as CNTs, the nucleation is likely to be random. On HOPG, it is hypothesized that with increasing numbers of deposition cycles, the LT AlO_x spreads out and extends over the uncovered terrace regions instead of accumulating at the nucleation sites. Here, AlO_xH_y/Al_2O_3 adheres more strongly to the HOPG than to itself when the thickness is sub 2 nm, and the temperature is sufficiently low that stoichiometric Al_2O_3 formation is inhibited. Such lateral growth after the initial nucleation persists until ~2 nm thick coverage (Figure 2**a**−**e**). Therefore, due to the small size, it is likely that on CNTs, the LT AlO_x adhesion process for a conformal film would occur in less than 10 cycles.

It has been proposed that the LT AlO_x nucleation is a reversible adsorption−desorption process and is dependent on the substrate temperature.[37] At low temperature, the rate of LT AlO_x nuclei desorption is expected to be low, consistent with the high surface coverage seen at both 50 and 60 °C. However, the desorption rate increases with temperature consistent with the data at 70 °C (Figure 3**b**). It is also possible that increasing the surface temperature could reduce the physisorption of the LT AlO_x on HOPG. However, as the temperature range for LT AlO_x deposition is similar on HOPG and MoS_2[37] such a sharp change in coverage after 10 cycles between 60 and 70 °C seems more likely to be consistent with desorption being the key process to induce the coverage changes.

3.2. DFT Simulation. The related dynamics of the proposed nucleation and growth mechanism are consistent with atomic simulations, as shown in Figure 4. Low-temperature TMA + H_2O ALD produces oxygen-rich AlO_x (see the XPS study below) which may contain hydroxyl groups as shown by the XPS study below. However, it is impossible to determine the exact stoichiometry and structure with great certainty using available analytical tools such as XPS. Therefore, a model system of Al_2O_3 was chosen since it has the highest heat of formation and, therefore, would be the least likely to spread out on the graphene surface. The particles consisted of 5 formula units of Al_2O_3, with an approximate size of 0.8 nm × 0.5 nm × 0.5 nm. The HOPG surface was modeled as a single sheet of graphene. Various placements of two LT AlO_x particles were simulated with side-by-side and top-down configurations, as shown in Figures 4**a**,**b**, chosen for optimization *via* density functional theory (DFT). The experimental system was made up of CNTs supported on quartz. This system was too complicated to model by DFT, so a model consisting of a single sheet of graphene was employed since it would capture the most challenging part of the nucleation process which is the spreading of the AlO_x on the CNT surface instead of island formation. This graphene model also reflects the situation along the length of CNT where the curvature of CNT has less impact on the nucleation process. A model consisting of a suspended CNT or a CNT on a quartz substrate would have required the use of an even larger unit cell when including all of the vacuum space and was not practical. Van der Waals forces between the LT AlO_x particles and the graphene surface were incorporated via a Grimme DFT-D2 correction. For defect-free HOPG and CNT, the Al_2O_3 particles do not interact with the substrate through covalent or ionic bonding but through physisorption necessitating careful modeling of the van der Waals forces. Further simulation details are included in Section 5 of the Supporting Information.

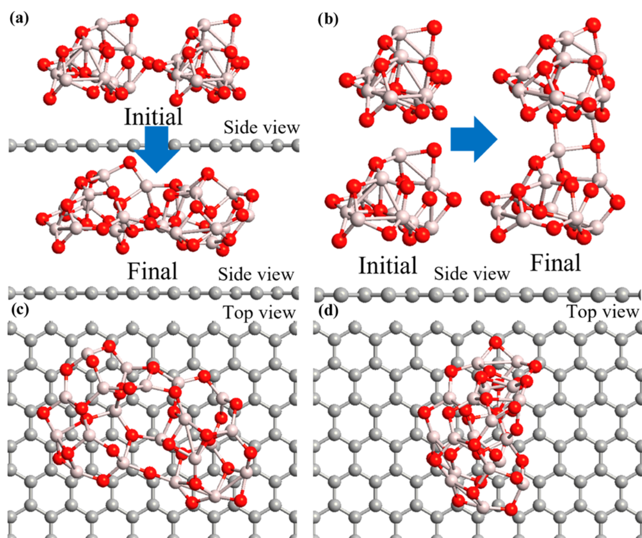

Figure 4. DFT simulation of Al_2O_3 cluster placement on a graphene sheet. The atomic configurations for (a) lateral and (b) stacked arrangements of the LT AlO_x cluster before and after DFT-based geometry optimization. The corresponding top-view of the final (c) lateral and (d) stacked configurations. The lateral configuration had lower total energy (~6.45 eV lower) compared to the stacked configuration. In the lateral case, the six oxygens in the Al_2O_3 clusters were closest to the graphene surface while the stacked configuration only allowed three to four oxygen atoms to be close to the surface. Furthermore, in the lateral configuration, nearly all of the Al atoms had a coordination number of 4, consistent with good thermodynamic stability.

During the optimization of the LT AlO_x adhesion onto the graphene surface, it was observed that the clusters preferred to spread out over the underlying hexagonal structure with the oxygen atoms in the LT AlO_x stabilized above the substrate carbon atoms, as shown in Figures 4**c**,**d**. This was unexpected since physisorption interactions between Al_2O_3 clusters and graphene are usually much weaker than the ionic bonding within Al_2O_3. However, very small Al_2O_3 clusters may have large bond strain, which affects the lowest energy configuration on graphene. It was observed that the Al_2O_3 clusters with the lowest energy configuration required a large atomic rearrangement of the oxygen atoms to the bottom of the cluster. Such rearrangement is the driver for the formation of flat, smooth Al_2O_3 films on graphene. Comparing the total energies of the optimized configuration, the lateral (side-by-side) configuration was 6.45 eV lower in energy compared to the stacked (top-down) configuration. Moreover, the binding energies, *i.e.*, the difference in energy when the LT AlO_x particles were faraway compared to when the particles were close to the graphene surface, for the lateral and stacked configurations were 2.26 and 1.48 eV, respectively. The larger binding energy of the lateral configuration is another indicator that LT AlO_x particles prefer to grow along the graphene surface, and is consistent with the observation of a uniform film thickness as a function of the ALD cycle number, as shown in Figure 2.

3.3. Electrical Measurement of Devices. For the characterization of the electrical performance of the LT AlO_x, related films were integrated with high-*k* oxides for fabricating bilayer dielectrics, which were then probed through MOSCAPs and FET device-based architectures, as indicated in

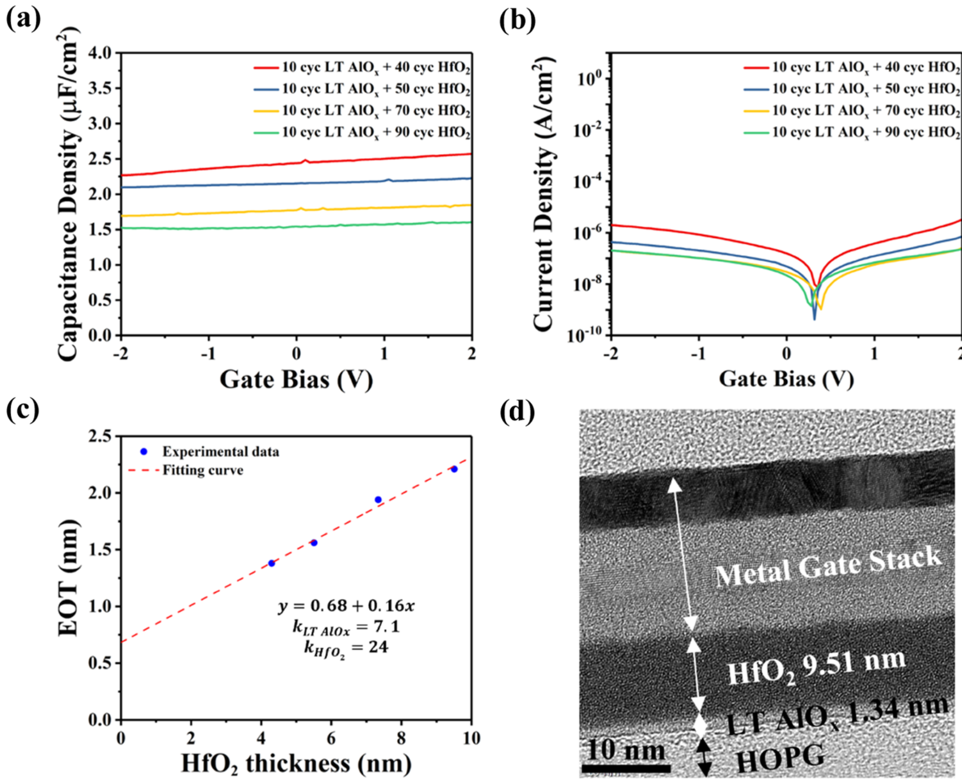

Figure 5. Experimental determination of k values for bilayer oxide with the gettering gate stack. (a) Capacitance per unit area at 100 kHz for various thicknesses of HfO_2 with a 2 nm LT AlO_x templating layer on HOPG. (b) Leakage current density for various thicknesses of HfO_2 on the sp^2 HOPG surface. (c) Equivalent oxide thickness (EOT) *vs* HfO_2 thickness. Extracted dielectric constant (k) values of LT AlO_x and HfO_2 were 7.1 and 24, respectively. (d) TEM of 10 cycles of LT AlO_x and 90 cycles of HfO_2 on HOPG. Reprinted with permission from ref 6 Copyright 2020 IEEE.

Figure 1. LT AlO_x was employed both to provide uniform nucleation and as a template for the deposition of various thicknesses of HfO_2. MOSCAPs fabricated using this bilayer gate oxide along with TiN/Ti/Pd gettering gates were characterized as shown in Figure 5. The C_{ox} values on HOPG decreased with increasing HfO_2 thickness as shown in Figure 5**a**. This was consistent with the C_{ox} being inversely dependent on the oxide thickness. Therefore, the maximum C_{ox} value of 2.5 $\mu F/cm^2$ was observed for the sample with 40 ALD cycles of HfO_2. Due to the inherent step edges of the HOPG substrate, lower cycles of HfO_2 oxides were unable to form a non-leaky device. A comparison of the $C-V$ results for the bilayer gate oxide deposited on a test Si substrate is shown in Figure S6, and exhibited similar thickness scaling, but the capacitance was lower due to the presence of a native SiO_2 layer. Owing to the insulating properties of the bilayer gate oxide, low gate leakage ($<10^{-5}$ A/cm^2 at +2 V) was observed for all samples on HOPG, as shown in Figure 5**b**. The capacitance of the bilayer dielectric is taken due to the series addition of the capacitances of LT AlO_x and HfO_2, *i.e.*,

$$\frac{1}{C_{\text{bilayer}}} = \frac{1}{C_{\text{LT AlO}_x}} + \frac{1}{C_{\text{HfO}_2}} \quad (1)$$

Assuming a parallel plate model, $C = kA/d$, with the dielectric permittivity k ($=k_o k_r$) with k_o as the vacuum permittivity ($=8.854 \times 10^{-14}$ F/cm) and k_r as the relative permittivity (or the dielectric constant), A as the electrode area and d as the distance between the electrodes, the EOT was calculated assuming equal A for all layers

$$\frac{\text{EOT}}{k_{\text{SiO}_2}} = \frac{t_{\text{LT AlO}_x}}{k_{\text{LT AlO}_x}} + \frac{t_{\text{HfO}_2}}{k_{\text{HfO}_2}} \quad (2)$$

The EOT ($=3.9/C_{\text{measurement}}$) was estimated, assuming the relative permittivity of k_{SiO_2} = 3.9, from the measured capacitance values on the devices represented in Figure 5**a**. From a plot of EOT *vs* t_{HfO_2}, with a known $t_{\text{LT AlO}_x}$, the values of the $k_{\text{LT AlO}_x}$ and k_{HfO_2} may be determined, from the intercept and slope, as indicated in Figure 5**c**. The t_{HfO_2} and the $t_{\text{LT AlO}_x}$ were determined through TEM, *e.g.*, as shown for the sample with 10 cycles of LT AlO_x (with $t_{\text{LT AlO}_x}$ − 1.34 nm) and 90 cycles of HfO_2 (t_{HfO_2} − 9.51 nm) in Figure 5**d**. The $k_{\text{LT AlO}_x}$ and the k_{HfO_2} were estimated as 7.1 and 24 for the LT AlO_x and HfO_2, respectively using a gettering gate.

To study the electrical properties of the LT AlO_x on CNTs, the bilayer oxide consisting of 4 cycles of LT AlO_x ($t_{\text{LT AlO}_x}$ − 0.35 nm in thickness) followed by 20 cycles of HfO_2 (t_{HfO_2} − 2.5 nm) was deposited on top of CNTs on quartz substrate (Figure 6**a**). The gate leakage device fabrication process is included in Section 1 of the Supporting Information. In contrast to HOPG where step edges are hundreds of nm apart, the CNTs have a diameter of ∼1 nm so LT AlO_x nucleation on CNTs is much easier, and fewer cycles of LT AlO_x are required. The physical thickness of the bilayer oxides after 4 deposition cycles of LT AlO_x and 20 cycles of HfO_2 with a non-gettering Ti/Pt gate was measured by TEM as 2.85 nm. Due to drawbacks of TEM imaging, the gate used in the TEM

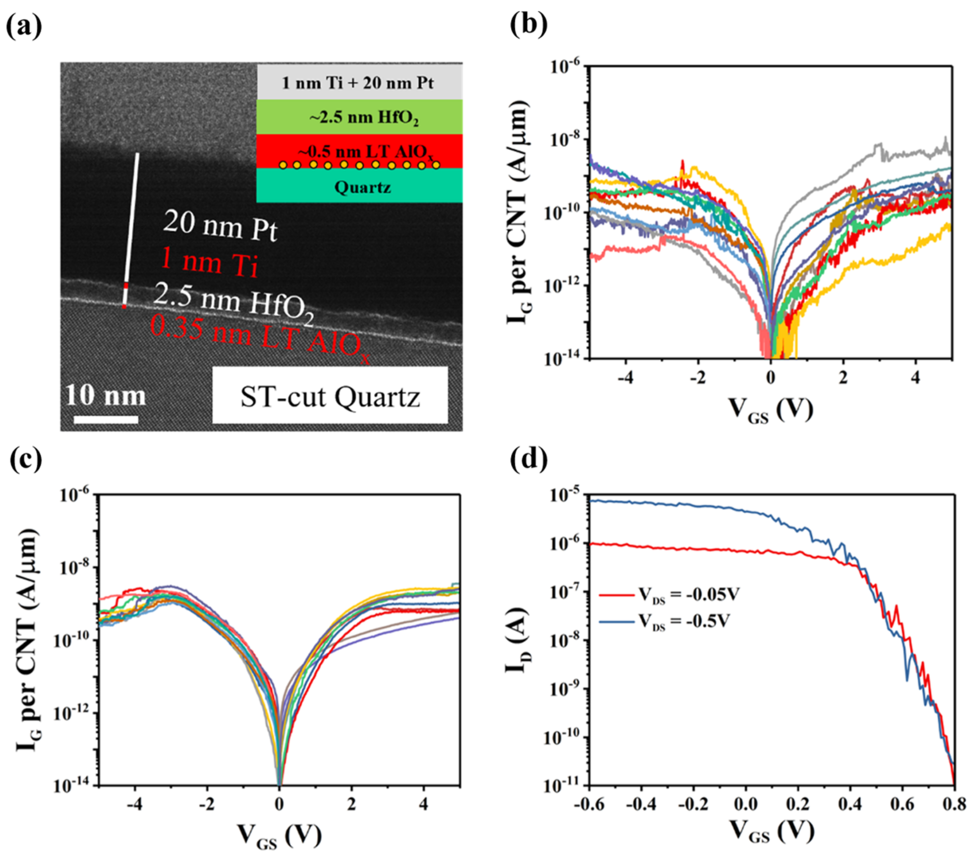

Figure 6. CNTFET gate leakage measurements with 4 cycles of LT AlO_x and 20 cycles of HfO_2. (a) HRTEM with 4 cycles of LT AlO_x and 20 cycles of HfO_2. (b) Gate leakage current for 4 cycles of LT AlO_x and 20 cycles of HfO_2 with non-gettering Ti/Pt gate metal. (c) Gate leakage current for 4 cycles of LT AlO_x and 20 cycles of HfO_2 with gettering TiN/Ti/Pd gate metal. (d) Transfer curves for 10 cycles of LT AlO_x and 20 cycles of HfO_2 with L_G = 100 nm Pd top gate.

imaging of the bilayer oxide on CNTs was 6 cycles of LT AlO_x and 20 cycles of HfO_2 and had a thickness of 3.15 nm, as shown in the Abstract. However, for gate leakage studies, a thinner gate of 2.85 nm fabricated with 4 cycles of LT AlO_x and 20 cycles of HfO_2 was employed. Using the previously extracted values for $k_{\mathrm{LT\ AlO}_x}$ and k_{HfO_2} of 7.1 and 24, with $t_{\mathrm{LT\ AlO}_x}$ and t_{HfO_2} assumed to be unchanged from the sample with non-gettering gate yields an estimated EOT according to eq 2 of ~0.6 nm. The measured $I-V$ characteristics for 20 devices with non-gettering Ti/Pt gate and gettering TiN/Ti/Pd gate are shown in Figure 6**b,c**, respectively. The gate leakage was less than 10^{-8} A/μm per CNT. While direct tests of mechanical stability were not preformed, good mechanical stability could still be inferred from the thin gate oxide being stable after full MOSFET fabrication. Such low gate leakage indicating only 4 cycles of LT AlO_x were required with additional 20 cycles of HfO_2 to achieve conformal coverage on CNTs. As a comparison, the work by Cavanagh et al.[30] showed that with NO_2/TMA treatment and additional 60 cycles of Al_2O_3 could achieve full coverage on CNTs. However, no $I-V$ transfer curve and gate leakage were discussed since MOSFET fabrication was not reported.

To study the performance of CNT transistors, top gate CNTFETs were fabricated with 10 cycles of LT AlO_x with additional 20 cycles of HfO_2, and a gate length 100 nm. The detailed process flow is also included in the Supporting Information Section 1. During the top gate measurement, the TiN back gate was used to apply a negative bias to the extension region for electrostatic doping to get a P−N−P carrier profile along the CNTs. Figure 6**d** showed a typical device that had a sub-threshold swing (SS) of 76 mV/dec. This result showed that the *SS* of LT AlO_x was lower than that of previously reported short-channel CNT devices with a gate oxide of 3 nm HfO_2[2]. Other researchers have already shown that lower SS corresponds to lower interface trap densities (D_{it})[8] with the corresponding equation is shown below. In the equation, q, k, T, and C_g are elementary charge, Boltzmann constant, temperature, and gate capacitance, respectively. Therefore, the low gate leakage and SS indicated that LT AlO_x had good electrical properties and mechanical stability.

$$\mathrm{SS} = \frac{\mathrm{d}V_g}{\mathrm{d}(\log I_{ds})} \approx 2.3\left(1 + \frac{qD_{it}}{C_g}\right)\frac{kT}{q} \tag{3}$$

3.4. Chemical Analysis. To compare the chemical state and the chemical composition between LT AlO_x and regular high-temperature Al_2O_3, both films were characterized by *ex situ* XPS as shown in Figure 7. All peaks were calibrated with the C 1s peak position at 284.8 eV, as shown in Figure 7**a**. For both LT AlO_x and high-temperature Al_2O_3, Al 2p peaks were symmetrically fitted to the peak at 74.4 eV, as shown in Figure 7**b**. For the LT AlO_x film, the O 1s peak was fitted with an asymmetric peak at 531.5 eV. After further deconvolution, one major peak was fitted at 531.1 eV, which indicated the Al−O bonds. Another small peak was fitted at 532.3 eV, which indicated Al−O−H hydroxyl groups, as shown Figure 7**c**. To verify that an OH component is present in the LT AlO_x, a

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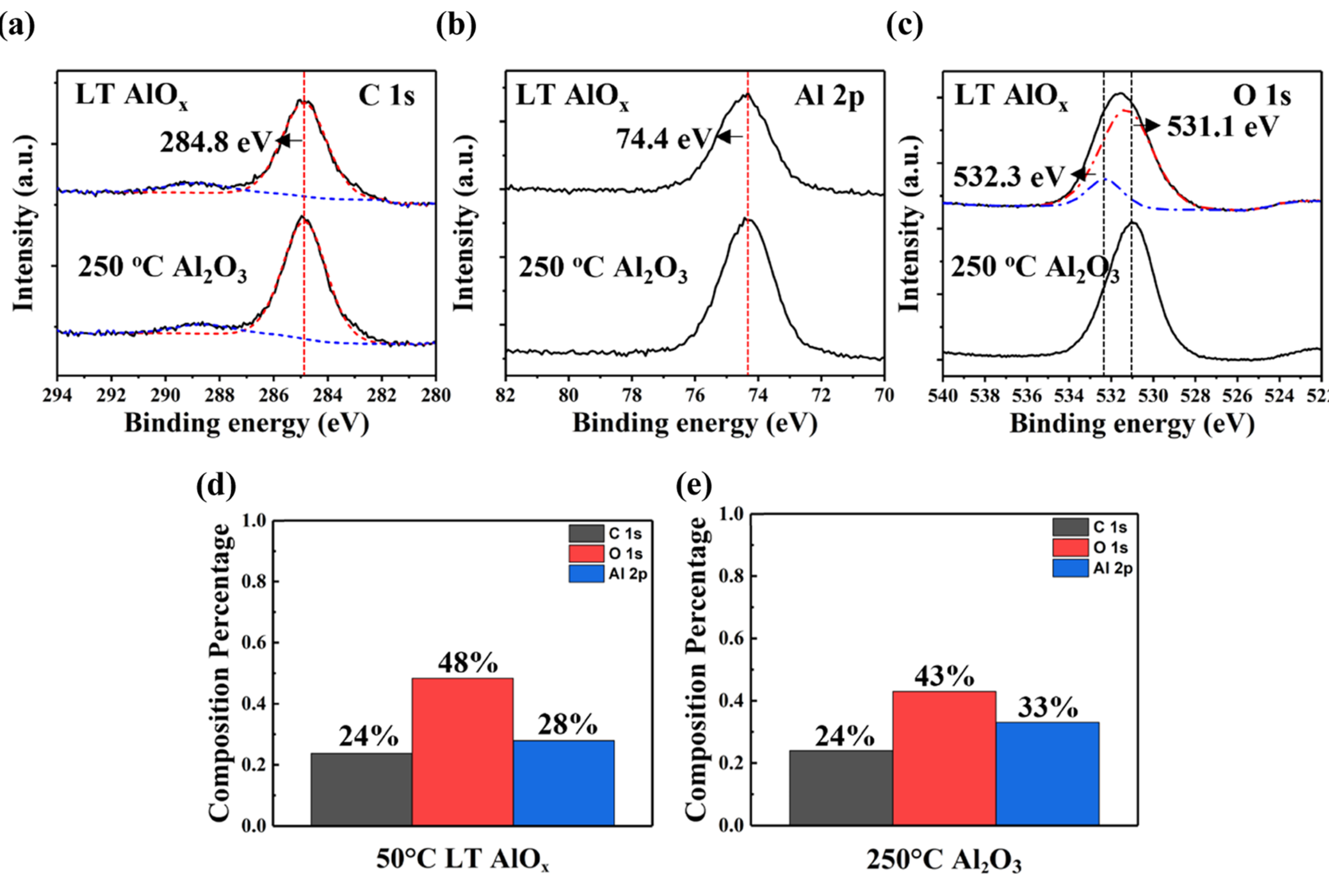

Figure 7. XPS spectra of LT AlO_x and 250 °C Al_2O_3. Comparison of high-resolution XP spectra of LT AlO_x and 250 °C Al_2O_3 of (a) C 1s, (b) Al 2p, and (c) O 1s. (d) Chemical composition of LT AlO_x. (e) Chemical composition of 250 °C Al_2O_3.

comparison was performed for fitting the O 1s with a 1-component fit *vs* a 2-component fit, as shown in Section 8 of the Supporting Information. The 2-component fit was clearly better than the 1-component fit; however, the Al 2p spectra for LT AlO_x and high-temperature Al_2O_3 had the Al 2p spectra with the same peak position and width; therefore, the charge states of the Al within the two films were similar. Such hydroxyl groups were generated by LT AlO_x deposition due to the combination of low purge time and low reaction temperature.[39] Both films were exposed to air prior to XPS and no Ar-ion milling was performed leading to the presence of ~20 at. % C, the majority of which was presumed to be adventitious carbon from air exposure. The O/Al ratio for 50 °C LT AlO_x was 1.7 while the O/Al ratio for 250 °C Al_2O_3 was 1.3, as shown in Figures 7**d**,**e**, respectively. These data were consistent with the result in Figure 7**c**, in which LT AlO_x was oxygen-rich. The LT AlO_x layer was characterized by XPS prior to the deposition of HfO_2. However, HfO_2 deposition can change the composition and structure of LT AlO_x by gettering oxygen and intermixing. The buried LT AlO_x layer, on the HOPG, was characterized by TEM. However, the LT AlO_x layer being sub 2 nm makes detailed TEM analysis very challenging. Instead, the layer was characterized by electrical measurements, which are sensitive to defect densities at the 1% level, involving film characterization not easily accomplished through TEM analysis.

4. CONCLUSIONS

The growth of sub-nanometer LT AlO_x on sp^2 carbon substrates was demonstrated by tuning precursor pulse time, purge time, and reaction temperature. AlO_x was deposited (2−10 cycles) on the HOPG substrate. The morphology of the depositions was studied by AFM to determine the growth mechanism. After the first several deposition cycles, AFM results showed that LT AlO_x grew laterally and achieved full coverage in 10 cycles on HOPG. Similar experiments were performed at substrate temperatures of 60 and 70 °C. The results showed that with higher temperature, the coverage of the film was reduced, consistent with the fact that higher substrate temperatures increase the desorption rate thereby lowering the coverage of AlO_x. To verify the growth mechanism, DFT simulations were performed which showed that lateral growth of Al_2O_3 on single-layer graphene had lower total energy (~6.45 eV lower) compared to the stacked configuration. To further investigate the electrical properties and stability of LT AlO_x, CNTFETs were fabricated. The electrical measurements of the CNTFETs showed 4 cycles of LT AlO_x with an additional 20 cycles of HfO_2 had a low gate leakage ($<10^{-8}$ A/μm per CNT) and an estimated EOT of 0.6 nm. A short-channel device using 10 cycles of LT AlO_x and 20 cycles of HfO_2 was measured and displayed a SS of 76 mV/dec, which indicated that the LT AlO_x layer had a low D_{it}. Therefore, the LT AlO_x process overcomes many of the obstacles for the deposition gate oxides on sp^2 carbon surfaces which should help enable the further advancement of carbon-based electronics.

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ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.1c21743.

Details of the CNTFET fabrication process, AFM morphology on HOPG at other temperatures, size distribution of the uncovered region for LT AlO_x deposition, C−V measurement of bilayer stacks on Si, EOT calculation, and DFT simulations (PDF)

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Notes

The authors declare no competing financial interest.

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