Bandgap Extraction at 10 K to Enable Leakage Control in Carbon Nanotube MOSFETs

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***Abstract*— Carbon nanotube (CNT) transistors exemplify the fundamental tradeoff between desirable high mobility and undesirable leakage current due to the small effective mass and bandgap. To understand leakage current limits in high-speed CNT transistors, electrical bandgaps are extracted on 12 single-CNT top-gate MOSFETs from the energy gap between thermionic emission and band-to-band tunneling (BTBT) at 10 K. At 300 K the minimum I_{OFF} at 0.5 V V_{DS} is analyzed as a function of bandgap between 0.96 eV and 0.43 eV with $I_{OFF\text{-}MIN}$ from 0.2 pA/CNT to 15 nA/CNT. NEGF simulation validates the bandgap extraction methodology and reproduces the experimental MOSFET $I_{OFF\text{-}MIN}$ data. A TCAD model calibrated to this work's leakage data projects the accessible I_{ON}-I_{OFF} design space bounded by CNT bandgap, indicating $E_G > 0.65$ eV ($d_{CNT} < 1.3$ nm) is needed to achieve 100 nA/μm at 0.5 V V_{DD} and 250 CNT/μm for channel length above 20 nm. An E_G of 1.06 eV ($d_{CNT} = 0.8$ nm) can deliver 2750× tunable range of I_{OFF} by adjusting V_T, which exceeds the 400× tunable range of I_{OFF} used in Si CMOS platform technologies.**

***Index Terms*— Carbon nanotube, CMOS, MOSFET, leakage current, band-to-band tunneling, bandgap extraction.**

I. Introduction

LOW-DIMENSIONAL semiconductor channel materials such as Carbon Nanotube (CNT) are potentially advantageous for CMOS logic beyond the 2 nm technology node. Recent advances have demonstrated essential transistor components such as 6.5 kΩ/CNT contact resistance at a 10 nm contact length [1], dense CNT assembly up to 250 CNT/μm [2], and short-channel effect immunity down to 15 nm gate length [3]. However, the dependence of leakage current on CNT bandgap has not been investigated by experiment. This work aims to (1) introduce a new method to extract the CNT bandgap based on electrical characterization of top-gate MOSFET structures at 10 K, (2) measure the limits of the leakage current for a large range of bandgaps in single-CNT MOSFETs, and (3) calibrate a TCAD CNT device model to project the range of tunable off-current between the limits of high-performance off-current density (~100 nA/μm) and band-to-band tunneling (BTBT) onset, with a view to identifying the range of CNT bandgaps suitable for logic platform technologies.

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II. Understanding the Leakage Challenge in Carbon Nanotube Transistors

High-speed compute and low-energy system-on-chip applications utilize granular standard cell-level control over transistor leakage by selecting high threshold voltage (V_{TH}) for non-critical path circuits, with selective use of low V_{TH} to meet timing requirements on critical paths. In Fig. 1(a) the I_D-V_{GS} for a typical CNT Schottky-barrier FET (SBFET) and CNT MOSFET are displayed, labeling: (1) I_{OFF} at $V_{GS} = 0$, (2) I_{ON} at $V_{GS} = V_{DS} = V_{DD}$, (3) I_{MAX} at largest $|V_{GS}|$, and (4) I_{MIN} at smallest measured I_D. I_{MIN} is the point beyond which any increase in V_{TH} does not reduce leakage current, and therefore is the key metric to evaluate the limits of energy-efficiency.

While previous literature [4]–[6] study mostly SBFET with gate overlapping source and drain contacts or asymmetric-SBFET with gate overlapping the source only, this work focuses on CNT MOSFET with doped source and drain extension region. Comparing MOSFET and SBFET, a MOSFET has (1) steeper above-V_{TH} transition to on-state which enables higher current at the same V_{DD} and I_{OFF}, (2) lower parasitic capacitance between the gate and contacts which enables faster switching, and (3) the band-to-band tunneling (BTBT) leakage mechanism that influences I_{MIN} in MOSFET is distinct from the ambipolar leakage mechanism which determines I_{MIN} in SBFETs, so should be considered separately. Fig. 1(b) explains the how BTBT (and thus I_{MIN}) is strongly influenced by channel material bandgap (E_G), however the correlation between I_{OFF} in CNT MOSFET and bandgap has not been previously reported [7]–[11].

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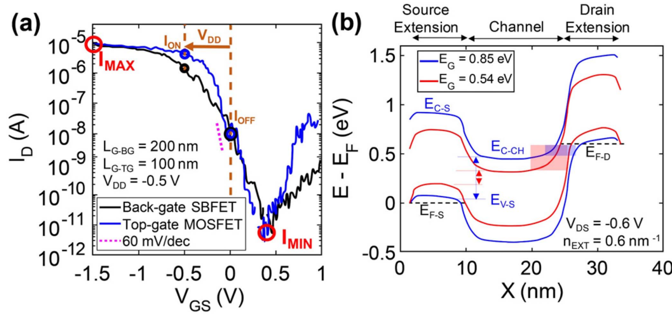

Fig. 1. (a) Example I_D-V_{GS} for single-CNT SBFET (black) and MOSFET (blue) from same CNT channel before/after top gate deposition [2]. The x-axis has been shifted to set I_{OFF} of 10 nA in both devices. (b) Band diagrams generated by TCAD simulation illustrate CNT MOSFET leakage sensitivity to bandgap (E_G). The vertical arrow on the source side indicates the energy transition required for source-to-channel BTBT. The highlighted region on the drain side indicates the energy range where BTBT may occur between the conduction band edge in channel ($E_{C\text{-}CH}$) and unoccupied states below the fermi-level in the drain valence band ($E_{F\text{-}D}$). At same bias conditions, smaller bandgap has larger BTBT due to both smaller source-to-channel energy transition and larger energy overlap between channel $E_{C\text{-}CH}$ and drain $E_{F\text{-}D}$.

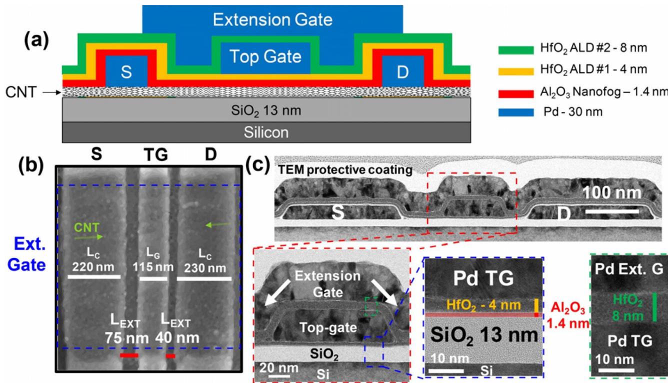

Fig. 2. Dual top-gate MOSFET device structure. (a) Cross-section schematic, (b) top-down scanning electron micrograph and (c) cross-section transmission electron micrograph of a typical device after fabrication. The 1.4 nm Al_2O_3 film is an interfacial oxide deposited by nanofog method [3]. All devices in this work have the same dimensions.

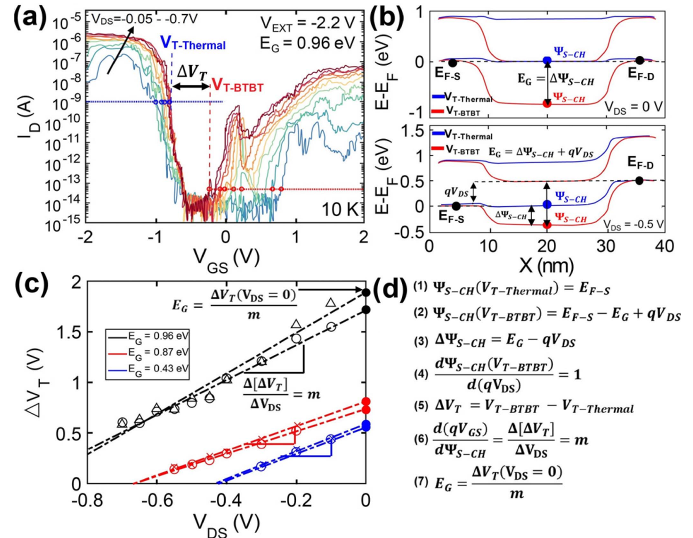

Fig. 3. (a) Bandgap extraction methodology begins with I_D-V_{GS} at 10 K. (b) Band diagrams corresponding to $V_{T\text{-}Thermal}$ (blue) when device enters subthreshold region and $V_{T\text{-}BTBT}$ (red) at onset of BTBT for V_{DS} of 0 V (top) and −0.5 V (bottom) for a $E_G = 0.85$ eV. (c) ΔV_T versus V_{DS} for multiple extension gate bias (V_{EXT}) to extract gate efficiency m, from linear regression slope and y-intercept at $V_{DS} = 0$. (d) Derivation of bandgap using parameters $\Delta V_T(V_{DS} = 0)$ and m found in (c). This approach is only valid if extensions are degenerately doped.

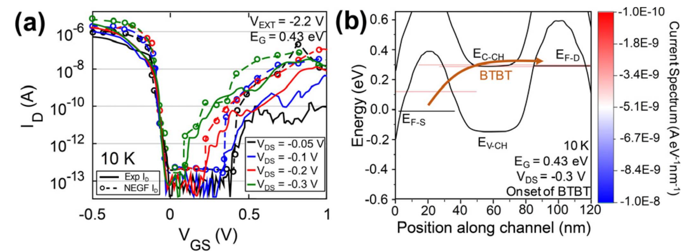

Fig. 4. (a) Comparison of NEGF-simulated and experimental I_D-V_{GS} for a CNT MOSFET of $E_G = 0.43$ eV at 10 K, showing good agreement in the onset of BTBT. (b) Band profile and position-resolved current spectrum at the onset of BTBT for $V_{DS} = -0.3$ V, showing main current contribution is BTBT while thermionic emission is negligible.

III. CNT MOSFET Bandgap Extraction

MOSFETs with single-CNT channels are fabricated on CVD-grown aligned CNTs with an intentionally broad diameter distribution ($d_{CNT} \sim 1.3$ nm, $\sigma_{CNT} \sim 0.4$ nm) [12]. A top-gate electrode modulates the channel potential, and an overlapping top-gate extension electrode is provided in this test structure to modulate the doping level in the extension (Fig. 2(a)). In a practical device technology, solid-state doping will be used instead of the extension gate [13]. Figs. 2(b,c) verify the device structure after fabrication and label all key dimensions.

To better understand how BTBT depends on the bandgap, a novel bandgap extraction method is developed as follows:

1. Measure I_D-V_{GS} at 10 K to clearly identify the onset of BTBT (Fig. 3(a)) by limiting the thermal tail. Repeat for multiple V_{DS}.
2. Define thermal branch threshold ($V_{T\text{-}Thermal}$) as device enters subthreshold region ($I_D = 1$ nA) and the tunneling branch threshold ($V_{T\text{-}BTBT}$) at onset of BTBT when I_D exceeds the noise level of 0.05 pA, corresponding to channel-source and channel-drain band alignments (Fig. 3(b)).
3. Fit $\Delta V_T = V_{T\text{-}BTBT} - V_{T\text{-}Thermal}$ versus V_{DS} with a linear function (Fig. 3(c)). The y-intercept represents the gate voltage swing to shift the channel surface potential at the valence band ($\Psi_{S\text{-}CH}$) exactly by E_G between these two thresholds at zero drain bias. The slope is the gate efficiency coefficient, which converts the gate voltage swing to channel surface-potential ($\Psi_{S\text{-}CH}$) as derived in Fig. 3(d).

NEGF modeling is used to validate the bandgap extraction method based on the same dual top gate structure. The simulation includes inelastic BTBT mediated by optical phonons [14], [15]. Due to computing limitations, a shorter gate length of 40 nm is used where direct source-to-drain tunneling remains negligible and the extracted bandgap is used as the input. Fig. 4(a) compares the experimental (solid lines) and NEGF-simulated I_D-V_{GS} curve (dashed lines) at 10 K, showing good agreement in $V_{T\text{-}BTBT}$ at the onset of BTBT. The bandgap extraction method is repeated on the NEGF-generated I_D-V_{GS} curves at 10 K and results in the same bandgap, further confirming the validity of this approach. The band diagram and current spectrum in Fig. 4(b) highlight the conduction path for phonon-assisted BTBT where carriers injected at the source

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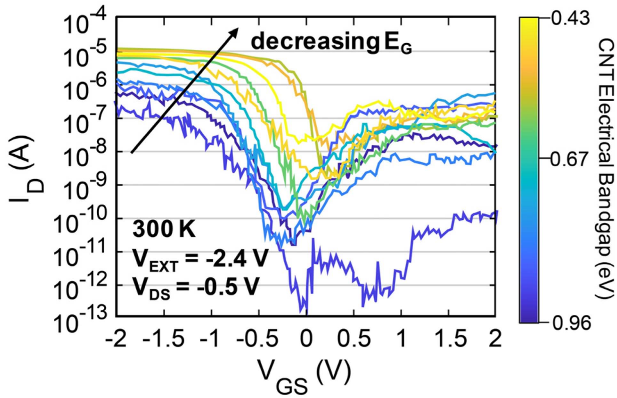


Fig. 5. I_D-V_{GS} at 300 K for 12 CNFETs with E_G = from 0.96 eV to 0.43 eV at −0.5V V_{DS}.

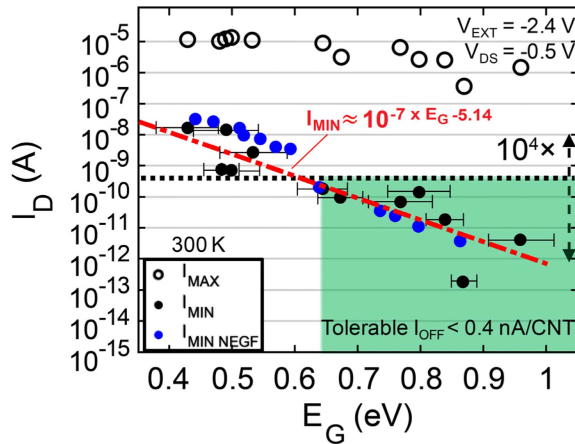


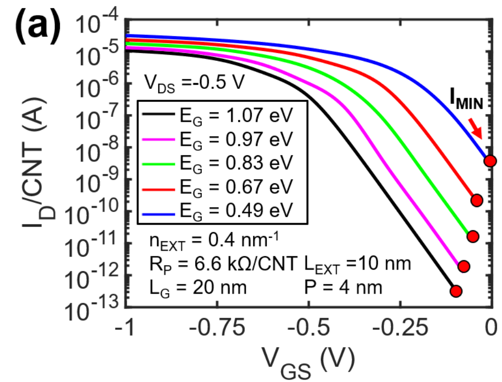
Fig. 6. Experimental I_{MIN} and I_{MAX} at 300 K versus E_G extracted for 12 single-CNT top-gate MOSFETs for V_{DS} = −0.5 V, showing good agreement with NEGF-simulated I_{MIN}. The I_{MIN} increases by ∼4 order of magnitude, while I_{MAX} only increases about 1 order of magnitude as E_G decreases from 0.96 eV to 0.43 eV. Large bandgap CNFETs have clearly demonstrated sub-10 pA/CNT 0.5V V_{DS}. Error bars indicate the uncertainty in the extracted bandgap accounting for the margin of error in the fitted slope, y-intercept, as well as the averaging effect from 3-5 repeated measurements.

can inelastically tunnel to the bounded states in the channel before tunneling to the drain.

IV. CNT MOSFET Leakage Analysis and TCAD Performance Projection

Fig. 5 shows the I_D-V_{GS} of 12 single-CNT MOSFETs. The extracted bandgaps range from 0.43 ± 0.05 eV to 0.96 eV ± 0.05 eV, which explain the significant difference in I_{MIN}at constant V_{DS}. Fig. 6 shows experimental I_{MIN} increases from sub-1 pA/CNT to more than 10 nA/CNT as E_G decreases from 0.96 eV to 0.43 eV at V_{DS} = −0.5 V at 300 K, with a good agreement from NEGF-simulated I_{MIN}. The CNT bandgap is inversely proportional to CNT diameter from band structure theory with tight-binding approximation and the diameter is determined by the (n, m) chirality of CNT [16]. Therefore, this data may guide future effort to control I_{MIN} and I_{OFF} variation through chirality and diameter selection [17].

The I_{MIN} data in previous section enables accurate TCAD-projected leakage behaviors for CNT MOSFETs. The TCAD model is calibrated with contact resistance, CNT density, and electrostatics that were experimentally demonstrated in the literature [1]–[3] and the I_{MIN} in this work. Fig. 7(a) shows the I_D-V_{GS} for 5 different bandgaps where the I_{MIN} is calculated



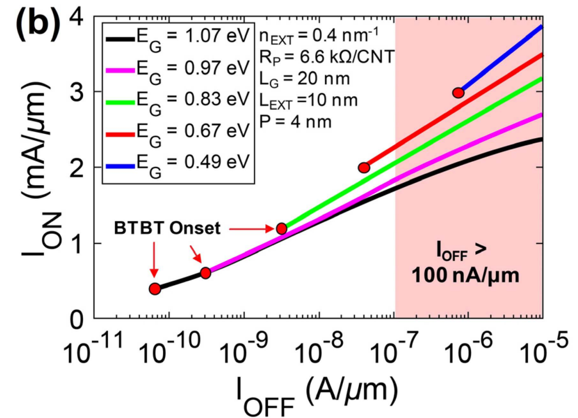


Fig. 7. (a) I_D-V_{GS} of CNFETs for 5 CNT bandgaps based on the TCAD model calibrated to this work's experimental I_{MIN} data, contact resistance R_P = 6.6 kΩ/CNT per contact [1], CNT density 250 CNTs/μm (pitch = 4 nm) [2], gate oxide capacitance from ref. [3], and moderate extension doping of 0.4 holes/nm. (b) TCAD projection of I_{ON}/μm versus I_{OFF}. Each curve represents accessible on/off current on the I_D-V_{GS}curve by V_{TH} shift with a window size V_{GS} = V_{DS} = V_{DD} for V_{DD} of 0.5 V.

based on the trendline in Fig. 6, fitted on the experimental data. Fig. 7(b) highlights the accessible off-current and on-current density between the lowest I_{OFF} limited by BTBT and a high-performance off-current specification of 100 nA/μm for a range of bandgaps at 0.5 V V_{DD}. The key new insights are (1) due to BTBT a very small design space exists for E_G ∼ 0.67 eV (d ∼ 1.27 nm), and CNT with even smaller bandgaps (larger diameter) have no design space at all at 0.5 V V_{DD}; (2) E_G ∼ 0.83 eV or larger (d_{CNT} ∼ 1 nm or smaller) tradeoff a linear decrease in I_{ON} with exponential improvement in device leakage, and (3) an E_G of 0.97 eV (d_{CNT} ∼ 0.88 nm) can achieve 330× range of accessible I_{OFF} which is comparable to Si CMOS platform technology [18].

V. Conclusion

In summary, a new methodology is developed to extract the CNT bandgaps in CNT MOSFETs based on electrical characterizations at 10 K. With this method, the CNT MOSFET leakage current is reported across a range of bandgap for the first time. NEGF simulation validates the bandgap extraction method and leakage current dependence on bandgap. This work also projects the on- and off-current achievable between limits of BTBT-onset and high leakage power. Future studies should investigate additional leakage from source-to-drain tunneling (SDT) below 20 nm L_G and utilize solid-state doping methods in the extension region.

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