Letters

Cu–Cu Bonding Using Selective Cobalt Atomic Layer Deposition for 2.5-D/3-D Chip Integration Technologies

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***Abstract*— The feasibility of using selective thermal cobalt metal (Co) atomic layer deposition (ALD) as high density Cu–Cu interconnect bonding is demonstrated at a low temperature (200 °C) and with minimal surface pretreatment. A Cu/Gap/Cu structure, which emulates 3-D ICs stacking is fabricated. Cobalt ALD showing seamless interconnection between copper (Cu) pads with 30-μm pitch is demonstrated with greater than 90% yield through electrical measurements, SEM inspection, EDS, and focused ion beam (FIB) cross section.**

***Index Terms*— Cu–Cu bonding, fine-pitch I/O, selective cobalt atomic layer deposition (ALD).**

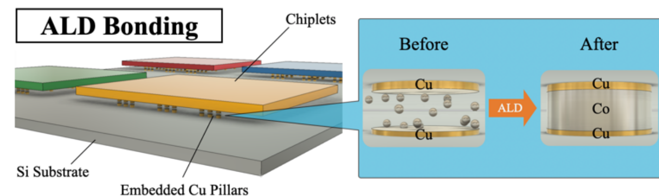

Fig. 1. Concept of ALD die bonding with multiple chiplets.

I. Introduction

AS MOORE'S Law slows down, 3-D chip integration will play an important role in the next generation of electronics as recently demonstrated by Intel's Foveros [1] and TSMC's SoIC [2] technologies. The 3-D integration technologies exhibit dense interconnections between chips, thus decreasing the transmission latency and power consumption, and increasing bandwidth density. The shorter interconnect distances afforded by 3-D IC integration also decreases the size of the package/microsystem by bonding multiple chips vertically within the same footprint.

Bonding technology is a key building block for 3-D integration and has evolved from board-level to chiplet-level bonding. Although the function of bonding has not changed, the smaller dimensions and material limitations have created significant challenges. For example, the semiconductor industry commonly uses tin-based solder for flip-chip bonding and microbump bonding with I/O pitches ranging from a few hundred micrometers to 50 μm [3]. However, when the bump pitch scales to approximately less than 40 μm, the solder bumps can easily short with adjacent bumps during bonding because the bumps are melted [4]. In addition, solder bumps can create unfavorable intermetallic compounds, which decrease the thermomechanical stability [5].

To address these challenges, prior work has explored Cu–Cu direct bonding for fine pitch interconnects. In the past two decades, several Cu–Cu direct bonding methods have been developed using, for instance, self-assembled monolayer bonding [6], surface activated bonding [7], and various Cu passivation methods [8]. However, most of these technologies utilize thermomechanical processes, which may require high temperatures, extreme surface planarities, high surface cleanliness, and large mechanical forces; these requirements present a number of challenges in the implementation of densely connected 3-D IC stacks.

Another important technology for dense bonding is hybrid bonding. This bonding method first performs direct bonding of the oxide layer that surrounds the Cu pads and subsequently forms Cu bonding with a low temperature anneal (150 °C–300 °C) [9]. The semiconductor industry has demonstrated sub-10 μm pitch hybrid bonding and has applied this technique to high-end semiconductor processes [10]. However, hybrid bonding requires a sophisticated chemical mechanical polishing (CMP) process to create precise planarization of Cu pads across the whole wafer [11]. In addition, the surface cleanliness and conditioning requirements along with tight alignment specifications may introduce difficulties as I/O pitches continue to scale aggressively in the future (sub-micrometer).

In this letter, a Cu–Cu bonding method for next-generation dense 3-D integration is proposed. For the first time, we propose and demonstrate a selective thermal atomic layer deposition (ALD) process for the formation of the I/Os. As shown in Fig. 1, the proposed selective thermal ALD process deposits Co only between the Cu pads to form interconnections when two (or multiple) chips that are stacked with small gaps. Once the ALD deposit grows to the thickness of the gap between the two dice, the Cu pads (or copper pillars) become interconnected.

ALD offers several advantages for ultradense bonding. First, ALD can control film thicknesses to the angstrom level, which theoretically can allow the bonding of I/Os at a nanometer scale. Second, ALD bonding does not require extreme Cu surface planarity or cleanliness,

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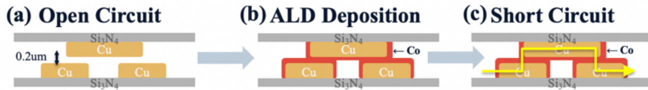

Fig. 2. Schematic of the Co ALD bonding design concept. (a) Before Co ALD deposition, the top and bottom copper pads are in open circuit. (b) During Co ALD deposition, the Co will grow on both sides of the copper pads. (c) After Co ALD deposition, the top and bottom copper pads are in short circuit through the grown Co.

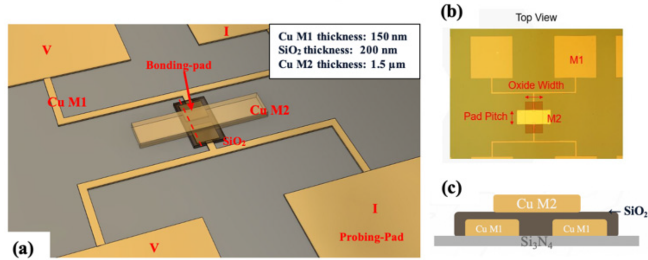

Fig. 3. Co ALD bonding testbed design. (a) 3-D CAD model. (b) Top view. (c) Cross section between bonding-pads (across dashed line).

which most thermal compression related methods and hybrid bonding require. Third, ALD bonding does not involve external mechanical forces, which can prevent die or wafer cracking. Fourth, ALD deposition is not affected by the size of the Cu pads, which means this technology can bond multidiameter and multipitch die pads simultaneously, which can be beneficial for signal and power/ground pads.

For this demonstration, selective-Co ALD is used because this process provides a low deposition temperature (150 °C–300 °C), an inherent selectivity to Cu surfaces over Si-based surfaces, and low resistivity. In this letter, a Cu/200-nm gap/Cu 3-D structure emulating 3-D stacked ICs is fabricated to demonstrate the proposed ALD I/O bonding method. Using the thermal selective Co ALD process, a seamless interconnection between pads with 30-μm pitch and 90% yield is shown.

II. EXPERIMENT

The concept of ALD bonding is shown in Fig. 2. In Fig. 2(a), before deposition, two parallel copper surfaces separated by a small gap form an open circuit between the Cu pads. In Fig. 2(b), after undergoing a selective thermal ALD process, the ALD deposit, which is Co in this case, grows only onto the Cu pads and gradually builds up from both pad surfaces until the Co deposits merge to form the interconnections. By measuring the resistance before and after deposition, the result demonstrates the process functionality.

The schematic of the test-bed which emulates the design concept of Fig. 2 is shown in Fig. 3, and the process flow is shown in Fig. 4. In Fig. 3(a), the first layer of Cu, M1, with 150-nm thickness, has two square-shaped bonding-pads in the middle and four probing pads at periphery. The M1 layer is fabricated by a physical vapor deposition (PVD) lift-off process with 150-nm-thick of Cu and 15-nm-thick of Cr adhesion layer, which is shown in Fig. 4(a). At the M1 layer, each bonding-pad is connected with two larger probing-pads. The size of the probing-pads is 200 μm × 200 μm, and the bonding-pads are 20 μm × 20 μm. By connecting the voltmeter and ammeter to the probing-pads on each side, as shown in Fig. 3(a), the four probing-pads form a four-point-measurement structure to characterize the resistance of the bonding-pads (and the short traces leading to them).

In Fig. 3(c), the M1 bonding-pads are covered with SiO_2 and the second layer of Cu, M2. The SiO_2 layer is 200-nm-thick and is fabricated by plasma enhanced chemical vapor deposition (PECVD),

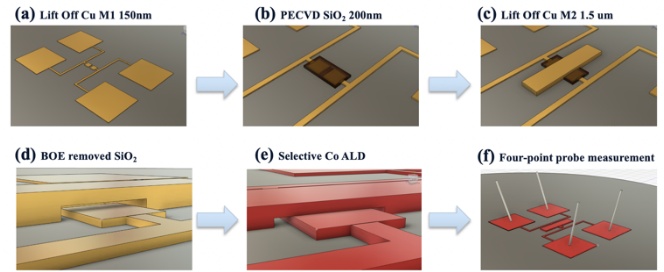

Fig. 4. Fabrication and experiment steps. (a) Lift off 150-nm-thick Cu M1. (b) PECVD deposit 200-nm-thick SiO_2. (c) Lift off 1.5-μm-thick Cu M1. (d) BOE etch of SiO_2. (e) Co ALD deposition. (f) Measurement.

TABLE I

RESISTANCE MEASUREMENT BEFORE AND AFTER Co ALD BONDING FOR 1000 CYCLES (" - ": THE FABRICATED TESTBED DID NOT YIELD)

Oxide Width (μm)	20	20	20	30	30	30	50	50	50	80	80	80	130	130	130	Ave
Pad Pitch (μm)	30	50	100	30	50	100	30	50	100	30	50	100	30	50	100	
Before ALD (Ω)	open	open	open	open	open	open	open	open	open	open	open	open	open	open	open	open
After ALD (Ω)	2.7	2.6	2.9	2.9	3.2	3.3	5.5	4.9	3.8	2.9	3.3	3.5	5.6	-	2.7	3.55

which is shown in Fig. 4(b). As shown in Fig. 4(c), the M2 layer consists of 1.5-μm-thick Cu and 15-nm-thick Ti adhesion layer, which are fabricated by a PVD lift-off process. In Fig. 4(d), SiO_2 is a sacrificial layer that will ultimately be etched away by buffered oxide etch (BOE) to create the gap between M1 and M2 layers before ALD deposition. In Fig. 5(b), a uniform 200 nm gap (in red dashed line) is shown after etching the sample in BOE for 10 min. The BOE etch removes the SiO_2 and the copper native oxide. M1 and M2 are characterized to make sure both sides of the copper surfaces are clean before ALD deposition.

Finally, a single chip with multiple interconnect designs is placed in a thermal ALD system for Co deposition. Before the ALD deposition, samples are annealed at 350 °C under ultra-high vacuum (UHV) to remove residue. The subsequent ALD process steps are Co $(DAD)_2$ (5.0 s)/turbomolecular pump down (10.0 s)/*tert*-butylamine (0.2 s)/turbomolecular pump down (10.0 s) at 200 °C; these steps are repeated for 1000 cycles to fill the 200-nm gap in the testbed. Each cycle grows approximately 1 Å of Co in a period of approximately 50 s. However, in a commercial ALD tool, the process would be faster. From the previous studies, within the 160 °C–220 °C ALD window, higher temperature will induce a faster Co deposition rate with virtually no change in resistivity [12]. The detailed mechanism of Co ALD deposition and precursor are well established [13]. Besides precleaning by 350 °C anneal, various methods of Co ALD deposition (e.g., formic acid, acetone ultrasonication) have been demonstrated at temperatures below 200 °C with great selectivity in previous studies [13], [14].

III. RESULT AND DISCUSSION

In Table I, the resistance of each interconnect design is measured before and after 1000 cycles of Co ALD deposition. The average resistance after Co ALD deposition is 3.55 Ω with a standard deviation of 1.07 Ω and the calculated ideal resistance is 1.85 Ω. From the resistance measurements, ALD Co bonding creates electrical pathways (i.e., interconnections) between M1 and M2 layers, and thus eliminates the open circuit.

To gain visual access within the gap, Kapton tape is employed to peel off the Cu M2 layer by repetitive peeling of a single 20 μm × 20 μm I/O. Using an optical microscope, Fig. 6(a) shows the top

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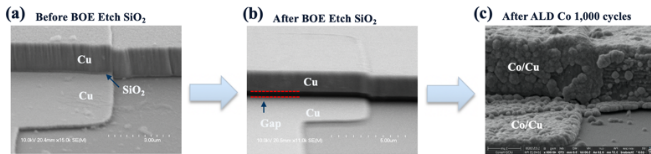

Fig. 5. SEM side view of testbed. (a) Before BOE etch of SiO_2 sacrificial layer. (b) After BOE etch of SiO_2 to create the 200-nm gap. (c) After 1000 cycles of Co ALD deposition.

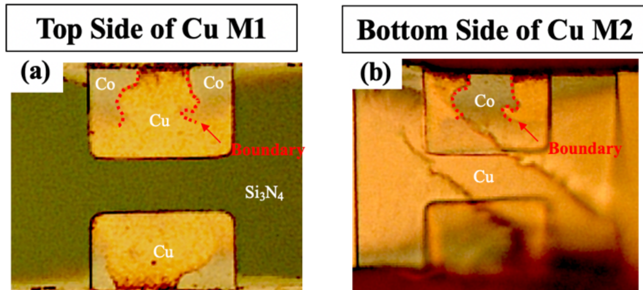

Fig. 6. Optical microscope image of bonding-pads after peel off Cu M2 layer. (a) Top side of Cu M1. (b) Bottom side of Cu M2.

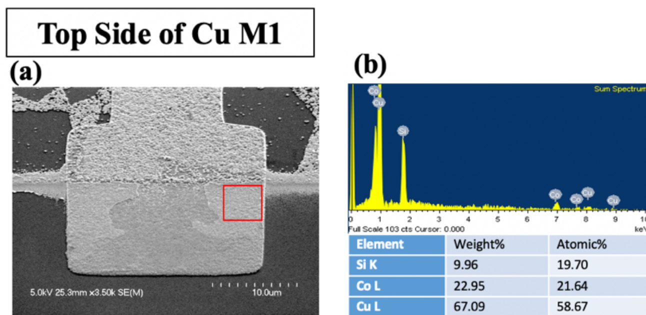

Fig. 7. (a) SEM characterization of the silver deposit on the bonding-pad after ALD Co deposition for 1000 cycles. (b) EDS reading of the red square area.

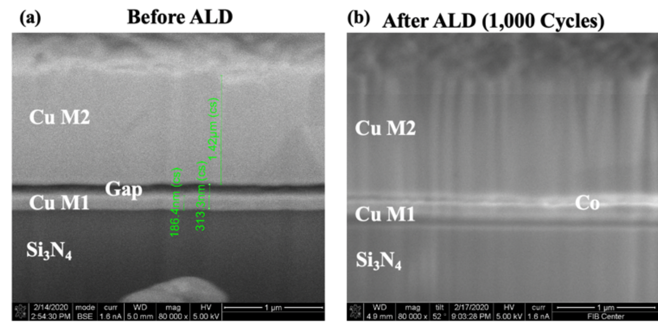

Fig. 8. FIB cross section across the bonding-pads. (a) Before ALD. (b) After ALD Co deposition 1000 cycles.

side of Cu M1 layer, and Fig. 6(b) shows the bottom side of the Cu M2 layer. These two sides face each other inside the gap. As shown in Fig. 6(a), the bonding-pads of Cu M1 layer are covered with Co deposit over half of each pad. To confirm, the sample in Fig. 6(a) is characterized by SEM and EDS, as shown in Fig. 7.

The geometrical form of the Co deposit is marked with the red dash boundary lines on Fig. 6(a) and (b). The boundary of Co in Fig. 6(a) matches the boundary of Co in Fig. 6(b). Comparison of the shapes of Co between Fig. 6(a) and (b) appears to be consistent with a full layer of Co being filled inside the gap before M2 was peeled off. EDS characterization was also used to characterize surface chemistry and confirm the deposition of Co on the peeled pads, as shown in Fig. 7(b).

To investigate further, focused ion beam (FIB) sputtering is employed to create a cross section of the ALD-bonded-pads and is observed by SEM. Fig. 8(a) shows an approximately 200 nm gap prior to selective Co ALD deposition between the pads. Fig. 8(b) shows the gap between the copper pads filled with Co ALD (after 1000 cycles) to create a seamless interconnection between Cu M1 and Cu M2.

The above data and measurements provide critical evidence of the feasibility of Co ALD for chip bonding. This new bonding method is not just limited to Co but is compatible with any thermal ALD deposition with high selectivity for growth of conductors (e.g., Mo, Ru, W) on metal substrates.

The main difference between the proposed ALD bonding technology and all other thermocompression related Cu–Cu direct bonding or hybrid bonding methods is that ALD bonding does not require metal diffusion to create the bond. ALD bonding deposits an intermediate layer between the Cu pads. In this way, ALD bonding does not need high temperature annealing, large mechanical force, extreme surface planarity, or cleanliness. Prior efforts in the literature also focused on creating an intermediate layer between copper pads/pillars using electroless plating. For example, Yang *et al.* [15] demonstrated that electroless Ni plating can bond Cu pillars at a low temperature. However, electroless plating may potentially not support fine pitch bonding due to the possible need of an external pump to circulate the solution into small gaps (i.e., between chips). Using an external pump is difficult to implement in a bonding process, especially in a batch-scale wafer process due to large pumping pressures. Conversely, selective thermal ALD is based on gas diffusion and gas-surface reactions enabling bonding at finer gaps and pitches than liquid phase precursors.

IV. Conclusion

For the first time, ALD bonding between Cu pads is demonstrated; the process is based on selective Co thermal ALD at low temperature (200 °C), requires low surface cleanliness from native copper oxide and low flatness, and requires no mechanical forces. A Cu/200-nm gap/Cu testbed was employed to emulate two chips stacked close together during bonding. By comparing the electrical resistance and FIB cross sections before and after Co ALD deposition, Co ALD demonstrated over 90% yield and created a seamless interconnection within 200 nm gaps Cu gaps at 30-μm pitch. This effort demonstrates the feasibility of ALD bonding; further work will focus on chip-scale mechanical strength analysis and explore the effective coverage under wafer-scale bonding.

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