Low-leakage WSe_2 FET gate-stack using titanyl phthalocyanine seeding layer for atomic layer deposition of Al_2O_3

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The fabrication of top-gated transition metal dichalchogenide (TMD) field-effect transistors (FETs), requires a uniform and pinhole-free gate dielectric. For realization of TMD tunnel FETs (TFETs) a high-k gate dielectric with subnanometer equivalent oxide thickness (EOT) is required. However, deposition of a thin, uniform high-k dielectric on a TMD surface without functionalization is challenging [1]. This is due to the lack of dangling bonds on the TMD surface. In this report, titanyl (TiO) phthalocyanine ($C_{32}H_{18}N_8$), TiOPc, is used successfully as a seeding layer on WSe_2 to enable the atomic layer deposition of Al_2O_3. TiOPc is an organic semiconductor with a band gap of approximately 2 eV in air [2]. We demonstrate the first top-gated TMD FET with an EOT as low as 2.2 nm ($\varepsilon_{Al2O3} = 9$) and a gate leakage current density of 0.2 pA/μm^2 at 1 V gate bias. The best prior report we have found, by Liu [3] on MoS_2, achieved an EOT of 6.9 nm with a gate leakage current density of 2 pA/μm^2. As a point of reference the ITRS [4] targets an ultimate EOT for CMOS approaching 0.4 nm with a current density below 0.25 pA/μm^2. Here, we compare the electrical characteristics of top-gated TiOPc-seeded Al_2O_3 WSe_2 FETs against the characteristics of the same transistor with an ALD Al_2O_3 back gate. We also report the improvements obtained by post-deposition high vacuum annealing.

The process flow consisted of electron-beam (EB) evaporation of Ti/Au (5/100 nm) on the back of a p^+ Si wafer. On the top surface, 27 nm of Al_2O_3 was next deposited by ALD. WSe_2 flakes (2D Semiconductors Co.) were then exfoliated on the 27 nm Al_2O_3 layer. The flakes were patterned for source/drain contacts using EB lithography (EBL) followed by EB deposition of Ti/Pd (0.8 nm/ 90 nm) and lift off. A monolayer of TiOPc was then deposited on the WSe_2 by organic molecular beam epitaxy [5]. Next, the ALD of 5 nm Al_2O_3 was performed at 120 °C. Finally, the top gate contacts were patterned using EBL, followed by EB deposition of Ti/Pd (0.8 nm/ 120 nm) and lift off.

The electrical characteristics of back gated and top gated devices were measured at 300 K in a vacuum probe station at a pressure of 1.9×10^{-6} Torr. The transistors showed a stronger current modulation with the back gate, 1000, compared to the top gate, 100, due to a reduction in contact resistance with the back-gate bias. High vacuum annealing (HVA) was performed on one transistor wafer at 200 °C at a pressure of 1×10^{-10} Torr for 10 minutes. The drain current increased by an order of magnitude in most of the transistors, whereas top and back-gate currents remained the same.

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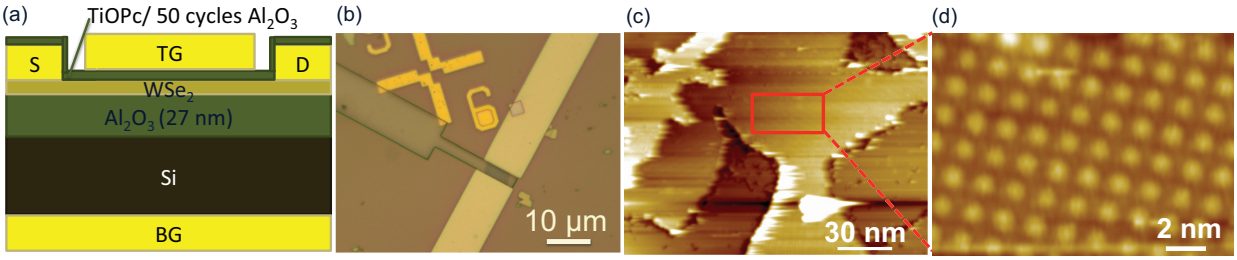

Figure 1 : (a) Schematic cross-section and (b) optical microscope image of a top gated WSe_2 FET with source-drain spacing $L_{SD} = 3$ μm and top gate length $L_{TG} = 2.8$ μm. (c) STM image of TiOPc/WSe_2. The TiOPc molecules form square lattice structure. (d) In the zoomed image, each center of the TiOPc molecule is seen as the bright O protrusion. Since O and N in TiOPc have localized charge density, they have high reactivity with the ALD precursors.

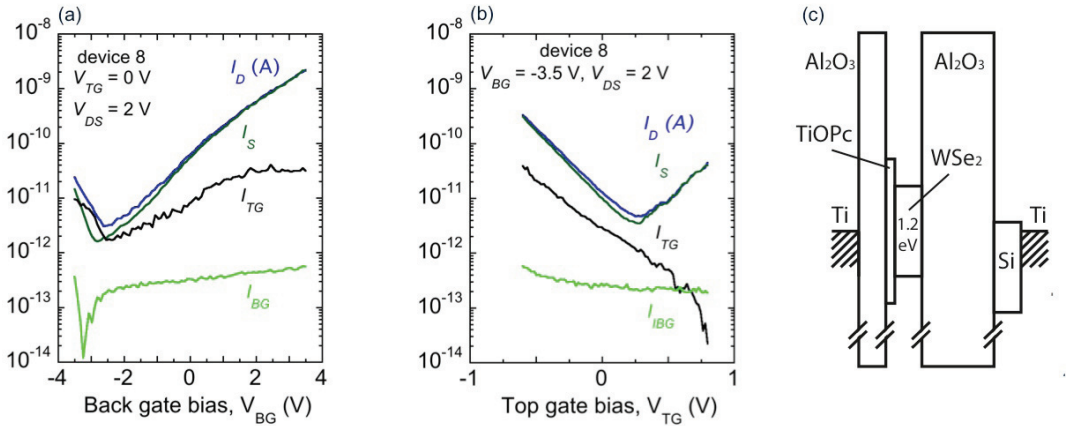

Figure 2: WSe_2 FET transfer characteristics under (a) back gate modulation and (b) top gate modulation ($L_{SD} = 3$ μm, $L_{TG} = 2.6$ μm, wafer F4). The back gate modulation is stronger than the top gate because the back gate has control over the entire channel and contacts, while the top gate controls only part of the channel. (c) Flat band diagram of the front and back gate structure in the vertical direction.

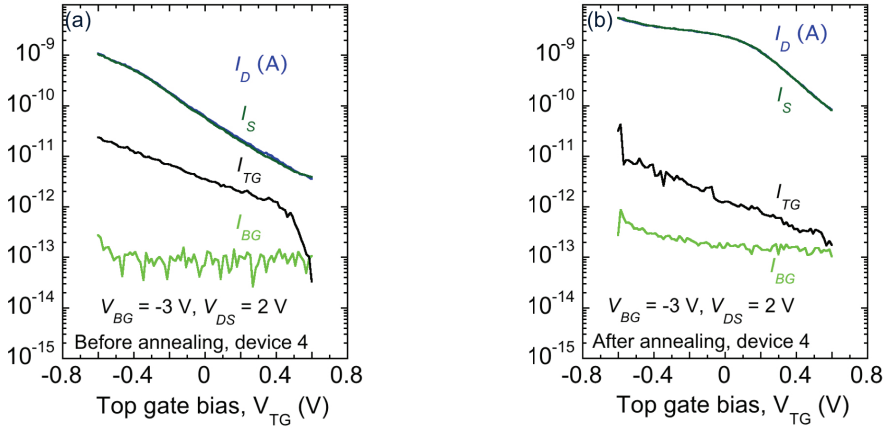

Figure 3: WSe_2 FET transfer characteristics with TiOPc/Al_2O_3/Ti/Pd gate stack ($L_{SD} = 2.1$ μm, $L_{TG} = 1.5$ μm, wafer F4): (a) before high vacuum annealing (HVA) and (b) after HVA. After HVA, the drain current increased by over an order of magnitude, while leakage currents decreased only slightly.