

Contents lists available at ScienceDirect

Applied Surface Science



journal homepage: www.elsevier.com/locate/apsusc

Full Length Article

Low interface trap density in scaled bilayer gate oxides on 2D materials via nanofog low temperature atomic layer deposition



Iljo Kwak^a, Mahmut Kavrik^a, Jun Hong Park^{a,d,e}, Larry Grissom^c, Bernd Fruhberger^c, Keith T. Wong^f, Sean Kang^f, Andrew C. Kummel^{b,*}

^a Materials Science and Engineering Program, University of California San Diego, La Jolla, CA 92093, United States

^b Department of Chemistry and Biochemistry, University of California San Diego, La Jolla, CA 92093, United States

^c California Institute for Telecommunications and Information Technology, University of California San Diego, La Jolla, CA 92093, United States

^d Center for Quantum Nanoscience, Institute for Basic Science (IBS), Seoul 03760, Republic of Korea

^e School of Materials Science & Engineering, Gyeongsang National University, Jinju 52828, Republic of Korea

^f Applied Materials, 974 E Arques Ave, Sunnyvale, CA 94085, United States

ARTICLE INFO

Keywords: Graphene Molybdenum disulfide (MoS₂) High-k dielectrics Density of interface states Electrical characterization Capacitance-voltage (C – V)

ABSTRACT

Al₂O₃ and Al₂O₃/HfO₂ bilayer gate stacks were directly deposited on the surface of 2D materials via low temperature ALD/CVD of Al₂O₃ and high temperature ALD of HfO₂ without any surface functionalization. The process is self-nucleating even on inert surfaces because a chemical vapor deposition (CVD) component was intentionally produced in the Al₂O₃ deposition by controlling the purge time between TMA and H₂O precursor pulses at 50 °C. The CVD growth component induces formation of sub-1 nm AlOx particles (nanofog) on the surface, providing uniform nucleation centers. The ALD process is consistent with the generation of sub-1 nm gas phase particles which stick to all surfaces and is thus denoted as nanofog ALD. To prove the ALD/CVD Al_2O_3 nucleation layer has the conformality of a self-limiting process, the nanofog was deposited on a high aspect ratio $Si_{N_4}/SiO_2/Si$ pattern surface; conformality of > 90% was observed for a sub 2 nm film consistent with a selflimiting process. MoS₂ and HOPG (highly oriented pyrolytic graphite) metal oxide semiconductor capacitors (MOSCAPs) were fabricated with single layer Al₂O₃ ALD at 50 °C and with the bilayer Al₂O₃/HfO₂ stacks having C_{max} of ~1.1 μ F/cm² and 2.2 μ F/cm² respectively. In addition, Pd/Ti/TiN gates were used to increase C_{max} by scavenging oxygen from the oxide layer which demonstrated C_{max} of ~2.7 μ F/cm². This is the highest reported Cmax and Cmax/Leakage of any top gated 2D semiconductor MOSCAP or MOSFET. The gate oxide prepared on a MoS_2 substrate results in more than an 80% reduction in D_{it} compared to a $Si_{0.7}Ge_{0.3}(001)$ substrate. This is attributed to a Van der Waals interaction between the oxide layer and MoS2 surface instead of a covalent bonding allowing gate oxide deposition without the generation of dangling bonds.

1. Introduction

2D materials such as graphene, MoS_2 and WSe_2 have attracted attention as future electronic devices due to their excellent electronic properties [1–10]. To switch on and off electric transistors, a few nanometer thick and defect-free gate oxide layers are integrated into the device fabrication for electrostatic gate control. However, due to the inert nature of the 2D material surfaces, the dielectric layers deposited by the conventional atomic layer deposition (ALD) processes preferentially nucleate at the defect sites or step edges. Such non-uniform oxides result in large leakage currents in the dielectrics of devices, consistent with the poor gate control [11–13]. Therefore, for successful integration of the 2D material devices, uniform and insulating gate oxides should be prepared. In order to deposit insulating gate oxides on 2D materials, various functionalization techniques have been studied such as surface treatment by using chemical solutions or $O_3(g)$, deposition of reactive metal or polymer-based seeding layers [12,14–19]. However, these chemical functionalization methods frequently induce damage to 2D materials, change the electronic properties of 2D materials, or the seeding techniques require complicated vacuum processes and thick dielectric layers. Therefore, a more facile low defect gate oxide deposition method is required for successful fabrication of 2D material-based devices.

In this work, aluminum oxide (Al₂O₃) was deposited on 2D material surfaces by low temperature ALD without any seeding layers or surface treatments. By controlling precursor pulse and purge times, a chemical

* Corresponding author.

E-mail address: akummel@ucsd.edu (A.C. Kummel).

https://doi.org/10.1016/j.apsusc.2018.08.034

Received 12 June 2018; Received in revised form 31 July 2018; Accepted 3 August 2018 Available online 10 August 2018 0169-4332/ Published by Elsevier B.V. vapor deposition (CVD) component was intentionally induced to form nucleation sites on the surface. The CVD growth component generated subnanometer AlOx particles on the 2D material surfaces forming uniformly deposited pinhole-free dielectrics; the substrate independent deposition is consistent with a gas phase formation of the subnanometer AlOx particles and thus is denoted as "nanofog". As a means to demonstrate the self-limiting process of the ALD/CVD Al₂O₃ nucleation layer, the 20 cycles of nanofog ALD was deposited on a high aspect ratio Si₃N₄/SiO₂/Si fin surface; 2 nm thick film with conformality (step coverage) of > 90% was achieved.

To obtain higher capacitance and lower equivalent oxide thickness (EOT) gate stacks, Al_2O_3/HfO_2 bilayer gate oxides were deposited on the 2D materials with both non-reactive and reactive gate metals. To study the surface morphology, atomic force microscopy (AFM) was employed. The electrical properties of the oxides were evaluated by measurements of capacitance-voltage and leakage currents of metal oxide semiconductor capacitors (MOSCAPs). The density of interface states (D_{it}) for MoS₂ MOSCAPs was approximately one order of magnitude lower compared to the D_{it} for Si_{0.7}Ge_{0.3}(0 0 1) MOSCAPs. This is attributed to a Van der Waals interaction between the oxide layer and MoS₂ surface instead of a covalent bonding allowing gate oxide deposition without generation of dangling bonds.

2. Materials and methods

2.1. Nucleation study of low temperature Al₂O₃ ALD on 2D materials

Bulk MoS₂ and highly oriented pyrolytic graphite (HOPG) samples (SPI supplies) were mechanically exfoliated by an adhesive tape. The samples were transferred into a commercial ALD reactor (Beneq TFS 200 ALD system) which has a hot wall, crossflow reaction chamber. The base pressure of the reaction chamber was 1 mTorr. For Al₂O₃ ALD, TMA and H₂O were employed as precursor gases. The Ar carrier gas was continuously flowed at 300 sccm (standard cubic centimeter). 50 cycles of ALD were deposited and each cycle consisted of a sequence of a TMA pulse, an Ar purge, a H₂O pulse, and an Ar purge in the temperature range of 50-200 °C. In order to study the growth rate and the conformality of the Al₂O₃ film, 13 cycles and 50 cycles of ALD were deposited at 50 °C on a hydrogenated silicon oxycarbide (H:SiOC) substrate and 20 cycles of the ALD were prepared on a high aspect ratio patterned sample with Si₃N₄/SiO₂/Si fins; both samples were supplied by Applied Materials. Prior to ALD, the hydrogenated silicon oxycarbide (H:SiOC) and the high aspect ratio patterned samples were degreased by dipping sequentially in acetone, isopropyl alcohol, and DI water for 30 s followed by high purity N2 drying. The cross section of each samples was investigated by TEM (Transmission Electron Microscopy).

2.2. Electrical properties of the low temperature ALD film on 2D semiconductors

MoS₂, HOPG and p-type Si_{0.7}Ge_{0.3}(0 0 1) MOSCAPs were fabricated to analyze the electrical properties of the oxide. Si_{0.7}Ge_{0.3}(0 0 1) samples were cleaned by dipping sequentially in acetone, isopropyl alcohol, and DI water for 30 s. The native oxide of Si_{0.7}Ge_{0.3}(0 0 1) was removed by cyclic HF cleaning by a 2% HF solution and DI water at 25 °C for 1 min in each solution for 2.5 cycles and finished with 2% HF clean [20]. After 50 cycles of Al₂O₃ ALD process at 50 °C, 30 nm thick Ni top contacts were deposited on top of the oxide using thermal evaporation. A stainless-steel shadow mask was used to prepare the circular Ni contact patterns to avoid possible contamination from lithography and lift-off techniques. The diameter of contacts for MoS₂ and HOPG devices was 50 µm and 150 µm for Si_{0.7}Ge_{0.3}(0 0 1) devices.

In addition, to achieve high capacitance, Al_2O_3/HfO_2 bilayer gate oxide stacks were deposited on MoS₂, HOPG and Si_{0.7}Ge_{0.3}(0 0 1) substrates. 7 or 10 cycles of Al_2O_3 were deposited at 50 °C as a seeding

layer. Afterward, 40 cycles of HfO₂ were grown on top of the Al₂O₃ layer at 300 °C using hafnium tetrachloride (HfCl₄) and H₂O as precursors. Note that between the Al₂O₃ and HfO₂ growth, the samples were stored in the load lock to avoid background oxidant exposure at high temperature. For HfO₂ ALD, each cycle consisted of a HfCl₄ and a H₂O pulse with Ar purges after each precursor dose. AFM was used in non-contact mode to characterize the surface topography after the ALD deposition.

Pd/Ti/TiN top contacts were also deposited on ALD dielectric to study the oxygen scavenging effects on the deposited oxides. The Pd/ Ti/TiN contacts were deposited by DC sputtering and the thicknesses of Pd/Ti/TiN layers were 30 nm, 30 nm and 5 nm respectively. The sizes of Pd/Ti/TiN were identical as Ni contacts. Using Agilent B1500A semiconductor Device Analyzer, the capacitance of the oxides was measured as a function of voltage in the frequency range of 2 kHz to 1 MHz at room temperature. Leakage current densities were also obtained in the range of -2 V to 2 V. The conductance method was applied to extract density of interface states (D_{it}) of MoS₂ and Si_{0.7}Ge_{0.3} MOSCAPs [21].

3. Results and discussion

3.1. Nucleation of Al₂O₃ on 2D materials

The effects of ALD temperature on nucleation of Al₂O₃ on HOPG were investigated. AFM images of Al2O3 ALD on HOPG using 50 cycles of ALD dielectrics in the temperature range of 50-200 °C are shown in Fig. 1. For the samples in Fig. 1(a)–(c), a 600 ms TMA and a 50 ms H_2O pulses were used with a 500 ms Ar purge time between the two precursor pulses. The nucleation of Al₂O₃ on HOPG was strongly dependent on the sample temperature. Typically, Al₂O₃ ALD is performed above 150 °C to reduce fixed charges in the oxide and interface defect density [22]. When the ALD was performed on HOPG at 200 °C and 150 °C (Fig. 1(a) and (b)), Al₂O₃ was only deposited at the step edges of the HOPG and not on the terraces because of a lack of dangling bonds on the HOPG surface. However, when the ALD temperature was decreased to 50 °C (Fig. 1(c)), the Al₂O₃ film was continuously grown on both the step edges and the terrace without formation of any visible pinholes. Round Al₂O₃ particles were observed across the entire surfaces at this temperature.

The height and diameter of the particles (Fig. 1c) was about 2 ± 0.4 nm and 20 ± 9.5 nm as quantified by line profiles in multiple AFM images. These particles are attributed to a CVD growth component. The short purge times for this study could induce the CVD reaction because of excess ALD precursors remaining in the gas distribution system. Under these conditions, TMA and H₂O can react with each other before reaching the substrate, and gas phase nucleation could occur to generate AlOx nuclei. It is hypothesized that the nuclei can be uniformly deposited on the surface by a reversible adsorption – desorption process due to the surface is covered with the nuclei, they eventually grow together and form a continuous Al₂O₃ film unlike the preferential nucleation in the case of Fig. 1(a) and (b). The asymmetric shape of the particles in Fig. 1(c) is consistent with agglomeration of weak bound, mobile sub 2 nm nuclei on the surface.

This proposed reversible adsorption–desorption nucleation mechanism would suggest that the nucleation behavior should depend on the substrate in the temperature range where the conformal AlOx nuclei deposition the surface can occur. To validate this hypothesis, identical 50 cycles of Al_2O_3 were deposited on a HOPG and a bulk MOS_2 substrates at different temperatures. Fig. 2 shows the AFM images of the surfaces of two different substrates After ALD. As shown in Fig. 2(a) and (d), similar Al_2O_3 nuclei were observed on the HOPG and the MOS_2 surfaces at 50 °C. However, at 80 °C, while Al_2O_3 was nucleated preferentially on the step edges and the defect sites on HOPG surface (Fig. 2(b)), a continuous film was grown only on the MOS_2 substrate (Fig. 2(e)). For an ALD temperature of 100 °C, Al_2O_3 film was



Fig. 1. AFM images of 50 cycles of Al_2O_3 films on HOPG with different ALD temperatures. (a) 200 °C; the ridges along the step edges are 4.5 nm tall; (b) 150 °C; the ridges along the step edges are 5.7 nm tall; (c) 50 °C; the height and diameter of the particles are 2 ± 0.4 nm and 20 ± 9.5. Each ALD cycle consisted of a 600 ms TMA pulse, a 500 ms Ar purge, a 50 ms H₂O pulse, and a 500 ms Ar purge.

discontinuous on both substrates (Fig. 2(c) and (f)). The different cutoff ALD temperatures on two substrates can be explained by the greater polarizability of the MoS₂ substrate compared to the HOPG substrate. The adsorption energy is expected to be higher with stronger surface polarizability providing strong dipolar interaction between the 2D semiconductors and the nuclei [23]. Graphene surface has weak polarization [13]; therefore, a lower ALD temperature is required for the nuclei to be deposited uniformly on a HOPG surface compared to the MoS₂ surface. There are two simple mechanisms to explain the formation of the Al₂O₃ particle layers on inert surfaces. (a) The TMA and the H₂O physisorb on the inert surfaces and form particles on the surface via reaction; (b) The TMA and the H₂O react in the gas phase and the particles reversibly deposit on the surface. Both processes are expected to be sensitive to pulse and purge times. The cutoff temperature for ALD being close to 100C is inconsistent with the physisorption mechanism of a purely surface based reaction; therefore, the temperature dependence is most consistent with gas phase nucleation in the ALD chamber [24]; therefore the technique is denoted as "nanofog" ALD.

The size of the ALD nuclei can be controlled by the ALD parameters enabling sub-1 nm RMS roughness oxides. Fig. 3(a) and (b) show the same 50 cycles of Al_2O_3 ALD on a HOPG and a bulk MOS_2 substrate with a 3 s purge. Compared to Fig. 2(a) and (d), the surface became significantly smoother consistent with smaller AlOx particles by increasing the purge time. This indicates that surface roughness can be controlled by purge times at this temperature.

Cross sectional TEM study was performed to investigate the conformality and the growth rate of Al_2O_3 ALD at 50C. Normally, a selflimiting process is documented in ALD by measuring the growth rate per cycle versus pulse time. However, for the ALD/CVD process, this is not possible because changing the pulse time changes the particle size. Instead, conformal deposition in a high aspect ratio sample with features below 50 nm was employed. Fig. 4(a) and (b) shows the TEM image of 50 cycles and 13 cycles of Al_2O_3 ALD on hydrogenated silicon oxycarbide (H:SiOC) substrates using a 200 ms of TMA pulse and a 50 ms of H_2O with 10 s of Ar purges between the pulses. As shown in Fig. 4(a) and (b), the Al_2O_3 films were uniformly deposited on the substrate. Average thickness of the 50 cycles and 13 cycles Al_2O_3 layers was 6.6 nm and 2.0 nm, therefore, the growth rates were 1.32 Å/cycleand 1.53 Å/cycle respectively. This growth rate is a slightly high growth rate compared to typical "pure" ALD growth rates (~1.1 Å/cycle) at high temperature and is attributed to the CVD component of the process [25,26]. Fig. 4(c) shows 20 cycles of Al₂O₃ ALD with the identical recipe as in Fig. 4(a), (b) on high aspect ratio Si₃N₄/SiO₂/Si fin structures (250 nm height \times 50 nm width, aspect ratio of 5:1). Conformality was quantity from the film thickness at the top of the sample compared to the bottom of the trench. Conformal 2 nm thick Al₂O₃ layer was deposited on the patterned structures without any visible pinholes. The growth rate was about 1 Å/cycle which is slightly lower than the ALD on a H:SiOC substrate due to the different material surfaces and structures. The conformality was determined to be 91% This result indicates ALD/CVD reaction was self-limiting consistent with the model of reversible adsorption/desorption of sub 1 nm Al₂O₃ particles formed in the gas phase. Similar conformality was also observed for nanofog deposition on 13 nm tall MoS₂ nanoribbons (Alessandri et al, IEEE Trans Elect Dev. 64(12), p 5217 (2017)) consistent with conformality on a sub 10 nm scale.

3.2. Electrical properties

Capacitance-voltage (C-V) and leakage current-voltage (I-V) of MOSCAPs with 50 cycles of Al_2O_3 at 50 °C were measured to evaluate the electrical properties of the oxide layer. Fig. 5(a)–(c) show the capacitance-voltage curves of MoS₂, HOPG and Si_{0.7}Ge_{0.3}(001) MOS-CAPs. In case of the HOPG in Fig. 5(b), the capacitance of the oxide was not dependent on the voltage. For a single layer of graphene, capacitance can be modulated near the Fermi level due to the linear dispersion of the density of states; conversely, due to the high charge carrier density of HOPG near the Fermi level, the modulation cannot be observed [27,28]. MoS₂ (Fig. 5(a)) and Si_{0.7}Ge_{0.3}(001) (Fig. 5(c)) samples showed n-type and p-type doping of the substrates. The negative flat band shift of MoS₂ sample was attributed to the charged defects on the surface, and the capacitance frequency dispersion in the accumulation region was due to the high series resistance of the bulk substrate. Note that the C_{max} of the three different samples was nearly identical (~1.1)



Fig. 2. AFM images and line profiles of 50 cycles of Al_2O_3 films on HOPG vs MoS₂. (a) HOPG 50 °C, (b) HOPG 80 °C, (c) HOPG 100 °C, (d) bulk MoS₂ 50 °C, (e) bulk MoS₂ 80 °C, (f) bulk MoS₂ 100 °C. The size of the images is $2 \times 2 \text{ um}^2$. The line profiles were taken along the red lines in each AFM image. Identical TMA, H₂O pulse and purge times as in Fig. 1 samples were employed. In the case of (b), (c) and (f), Al_2O_3 was only deposited at the step edges or defect sites on the surface. The ridges along the step edges are 4.5 nm, 5.1 nm, and 4.5 nm respectively. The height of oxide was about 5 nm consistent with 50 cycles of ALD. In the case (a), (d) and (e), Al_2O_3 was uniformly deposited. The heights AlOx particles were 2 ± 0.4 nm, 1.5 ± 0.2 nm and 2.1 ± 0.3 nm and the diameters were 20 ± 13 nm, 16 ± 8 nm and 35 ± 18 nm respectively.

 μ F/cm²) which is consistent with the reported values for 50 cycles of Al₂O₃ [29]. This indicates that growth rate of the oxide on the three substrates was nearly identical without an induction period.

The D_{it} was evaluated via the conductance method from the G-V data which is shown in Fig. 5(e) and (f) [21]. The conductance (G) is measured as a function of frequency and plotted as G/ω versus ω . G/ω

has a maximum at $\omega = 2/\tau$ and, at this frequency, the maximum $D_{it} = 2.5~G/q\omega$ can be determined. The details of the model and G/ω versus ω curves of the MoS₂ and SiGe MOSCAPs (Fig. S2) are included in the supporting information. As shown in Fig. 5(a) and (c), the D_{it} of MoS₂ MOSCAPs (9.84 \times 10¹¹ eV⁻¹ cm⁻²) is approximately one order of magnitude lower compared to the D_{it} of Si_{0.7}Ge_{0.3}(0 0 1) MOSCAPs



Fig. 3. AFM images and line profiles of 50 cycles of Al_2O_3 films with long (3 s) purge times on (a) HOPG and (b) bulk MoS₂ with. The size of the images is 2×2 um². The line profiles were taken along red lines in each AFM images. The 50 ALD cycles consisted of a 600 ms TMA pulse, a 3 s Ar purge, a 50 ms H₂O pulse, and a 3 s Ar purge at 50 °C. The height and diameter of the largest AlOx particles were 2.1 ± 0.2 nm and 2.2 ± 0.3 nm, but note that the surface has a roughness below 1 nm consistent with most particles being sub 1 nm diameter. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

 $(6.89 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2})$. This is attributed to a Van der Waals bonding between the oxide layer and the MoS₂ surface instead of a covalent bonding between the oxide layer and the Si_{0.7}Ge_{0.3}(001) surface. Fig. 5(d) shows the leakage current of the three samples. The leakage current densities of MoS₂, HOPG and Si_{0.7}Ge_{0.3}(001) samples were $2.2 \times 10^{-5} \text{ A/cm}^2$, $3.01 \times 10^{-5} \text{ A/cm}^2$ and $2.2 \times 10^{-6} \text{ A/cm}^2$ at -1 V. The slightly lower leakage of the Si_{0.7}Ge_{0.3} MOSCAPs is consistent with dangling bonds on the surface providing better nucleation of Al₂O₃. The low leakage current of the HOPG and MoS₂ devices indicates that the deposited oxides are uniform and pinhole free on the 2D materials.

To obtain higher capacitance with lower EOT, HfO_2/Al_2O_3 bilayer gate stacks were prepared using a two-step ALD method. First, 7 cycles of Al_2O_3 were deposited at 50 °C as a seed layer. Afterwards, the ALD reactor temperature was increased to 300 °C and, using $HfCl_4$ and H_2O

as precursors, 40 cycles of HfO_2 ALD were deposited on top of the Al_2O_3 . Note that the samples were stored in the load lock during the ALD reactor temperature change to avoid substrate damage. For comparison, identical oxides were deposited on MoS_2 , HOPG and $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$. The identical device fabrication process that was used for the pure Al_2O_3 MOSCAPs was employed.

Fig. 6 shows the electrical properties of MOSCAPs of MoS₂, HOPG and Si_{0.7}Ge_{0.3}(0 0 1) substrates with the Al₂O₃/HfO₂ bilayer stacks. As shown in Fig. 6(a)–(c), the C_{max} value was increased by factor of two (~2 μ F/cm²), compared to that of 50 cycles of Al₂O₃ due to the higher dielectric constant of HfO₂ as compared to Al₂O₃. The identical C_{max} value for the different substrates is consistent with identical growth rates and no significant induction period during the ALD. Fig. 6(d) is the leakage current measurement of the MOSCAPs. The leakage currents of the three samples indicates the oxides are insulating and uniform on



Fig. 4. (a), (b) TEM images of 50 cycles and 13 cycles of Al_2O_3 ALD on hydrogenated silicon oxycarbide (H:SiOC) substrates. (c) TEM image of 20 cycles of Al_2O_3 ALD on high aspect ratio Si3N4/SiO₂/Si fin structures. The black outmost layer is Al_2O_3 . The ALD cycles consisted of a 200 ms TMA pulse, a 10 s Ar purge, a 50 ms H₂O pulse, and a 10 s Ar purge at 50 °C.



Fig. 5. Capacitance vs. Voltage Curve of Ni/Low temperature Al_2O_3 50 ALD cycles on (a) MoS_2 , (b) HOPG, (c) $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$ substrates. (d) Leakage current density of Ni/Low temperature Al_2O_3 50 ALD cycles on MoS_2 , HOPG, $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$ substrates. (e), (f) Conductance density vs gate bias of MoS_2 and $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$ gate stacks respectively. Al_2O_3 ALD cycles consisted of a 600 ms TMA pulse, a 500 ms Ar purge, a 50 ms H_2O pulse, and a 500 ms Ar purge.

both 2D materials and Si_{0.7}Ge_{0.3}(0 0 1) substrate. However, the leakage current of MoS₂ MOSCAP was about 2 orders of magnitude higher at -1V compared to the other substrates. This is due to the high density of tall step edges (~10 nm tall) on bulk MoS₂ substrates. Due to the high aspect of the step edges, conformality of the oxide on the MoS₂ is expected to be less than on either HOPG or Si_{0.7}Ge_{0.3}(0 0 1) substrates resulting in the higher leakage. The D_{it} was evaluated using the conductance method from the G-V data in Fig. 6(e) and (f). The extracted D_{it} value of the MoS₂ MOSCAP was 8.9 × 10¹¹ eV⁻¹ cm⁻², which is about an 85% reduction compared to the D_{it} value of Si_{0.7}Ge_{0.3}(0 0 1) (5.89 × 10¹² eV⁻¹ cm⁻²) consistent with the result in Fig. 5. Employing low temperature ALD of Al₂O₃ as a seed layer, HfO₂ can be readily deposited on the inert surfaces of MoS₂ and HOPG while maintaining low leakage current.

It is known that titanium and titanium nitride (TiN) gates can be used to reduce the thickness of interface oxide layer in the Si, SiGe, and InGaAs MOSCAPs by gettering oxygen from the interface [30–34]. The

effect of the oxygen scavenging by Ti/TiN metal contacts on the HfO₂/ Al₂O₃ bilayer gate oxide was investigated using Pd/Ti/TiN, as shown in Fig. 7. Pd/Ti/TiN top contacts were deposited on the HfO₂/ Al₂O₃ bilayer oxide (40 cycles of HfO₂ at 300 °C/10 cycles of Al₂O₃ at 50 °C) by DC sputtering. Identical oxides and gates were deposited on MoS₂, HOPG and Si_{0.7}Ge_{0.3}(0 0 1) and capacitors were fabricated using the same process except the top contacts.

Fig. 7(a)–(c) present the capacitance-voltage measurements. The C_{max} of the three capacitors was increased to ~2.7 μ F/cm² which was about 30% higher compared to the HfO₂/Al₂O₃ bilayer stack with Ni Gate in Fig. 6. This improvement suggests that Pd/Ti/TiN gates scavenge oxygen from the gate oxide resulting in an increase of dielectric constant of the layer or thinner interface oxide layer (for SiGe). The C_{max} of the Si_{0.7}Ge_{0.3}(0 0 1) MOSCAPs was higher (~3.0 μ F/cm²) compared to MoS₂ and HOPG. This indicates that the oxygen scavenging is more effective on Si_{0.7}Ge_{0.3}(0 0 1) than MoS₂ and HOPG since there is an SiGeO_x interlayer. The D_{it} values from the MoS₂ and



Fig. 6. Capacitance vs. Voltage Curve of Ni/HfO₂ (40 ALD cycles)/Low temperature Al_2O_3 (7 ALD cycles) on (a) MoS_2 , (b) HOPG, (c) $Si_{0.7}Ge_{0.3}(0 \ 0 \ 1)$ substrates. (d) Leakage current density of Ni/HfO₂ (40 ALD cycles)/Low temperature Al_2O_3 (7 ALD cycles) on MoS_2 , HOPG, $Si_{0.7}Ge_{0.3}(0 \ 0 \ 1)$ substrates. (e), (f) Conductance density vs gate bias of MoS_2 and $Si_{0.7}Ge_{0.3}(0 \ 0 \ 1)$ gate stacks respectively. Al_2O_3 ALD cycles consisted of a 600 ms TMA pulse, a 500 ms Ar purge, a 50 ms H₂O pulse, and a 500 ms Ar purge. HfO₂ ALD consisted of a 500 ms HfCl₄ and a 500 ms H₂O pulse with a 6 s Ar purge.

 $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$ MOSCAPs are shown in Fig. 7(a) and (c). The D_{it} value of MoS_2 MOSCAPs was $1.12\times 10^{12}\ eV^{-1}\ cm^{-2}$ which is 88% lower than that of $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$ MOSCAPs (9.12 $\times 10^{12}\ eV^{-1}\ cm^{-2}$) consistent with the results in Figs. 5 and 6. Fig. 7(d) shows the leakage current measurement of three MOSCAPS. The leakage current densities of the three samples were similar to the results in Fig. 6 indicating lower EOT was achieved without degradation of the oxide layers.

4. Conclusion

In this study, deposition of high quality Al₂O₃ and HfO₂/Al₂O₃ films on 2D materials using low temperature ALD/CVD was demonstrated without organic seeding layers or chemical treatments. During ALD/CVD, AlO_x particles of below 1 nm diameter were formed on MoS₂, HOPG and Si_{0.7}Ge_{0.3}(0 0 1) consistent with a gas phase reaction of the ALD precursors to form sub 1 nm particles (denoted as nanofog) which reversible adsorb onto the substrates. The particles provided nucleation centers for further ALD on the inert 2D material surfaces. To document the nanofog process was conformal even on inert surfaces, a high aspect ratio Si₃N₄/SiO₂/Si structure was coated with sub 2 nm thick nanofog Al₂O₃ and was found to be 91% conformal. C_{max} and leakage current values of 50 cycles of low temperature ALD Al₂O₃ on MoS₂, HOPG and

 $\rm Si_{0.7}Ge_{0.3}(0~0~1)$ were comparable indicating uniform and pinhole free $\rm Al_2O_3$ films across the entire surface. In order to obtain lower EOT, $\rm Al_2O_3$ (7 cycles at 50 °C)/HfO_2(40 cycles at 300 °C) bilayer gate stack was prepared on 2D materials substrates. $\rm C_{max}$ was increased by $2\times$ compared to 50 cycles $\rm Al_2O_3$ MOSCAPs. Pd/Ti/TiN gate was employed to scavenge the oxygen from the oxide. $\rm C_{max}$ of $\sim 2.7~\mu F/cm^2$ was achieved with MoS_2 and HOPG without loss of leakage current density. All MoS_2 MOSCAPs in this study had lower interfacial defect density (D_{it}) compared to the same gate stacks on Si_{0.7}Ge_{0.3}(0~0~1) indicating Van der Waals interactions between the oxide and the 2D material surfaces was dominant instead of direct formation of covalent bonding. This study can provide a way to prepare superior interface of 2D semiconductor oxide gate stacks with low EOT and leakage current.

Acknowledgements

This work is supported in part by the National Science Foundation Grant DMR 1207213, by the Center for Low Energy Systems Technology (LEAST) and Applications and Systems driven Center for Energy-Efficient Integrated NanoTechnologies (ASCENT). STARnet and JUMP sponsored by Semiconductor Research Corporation (SRC) programs and DARPA, and by the SRC Nanoelectronic Research initiated



Fig. 7. Capacitance vs. Voltage Curve of HfO₂ (40 ALD cycles)/Low temperature Al_2O_3 (10 ALD cycles) with Pd/Ti/TiN contact of (a) MoS₂, (b) HOPG, (c) $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$ substrates. (d) Leakage current density of Pd/Ti/TiN/Low temperature $Al_2O_3(10\ ALD\ cycles) + HfO_2$ (40 ALD cycles) on MoS₂, HOPG and $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$ substrates. (e), (f) Conductance density vs gate bias of MoS₂ and $Si_{0.7}Ge_{0.3}(0\ 0\ 1)$ gate stacks respectively. $Al_2O_3\ ALD\ cycles$ consisted of a 600 ms TMA pulse, a 500 ms Ar purge, a 50 ms H₂O pulse, and a 500 ms Ar purge and HfO₂ ALD consisted of a 500 ms HfCl₄ and a 500 ms H₂O pulse with a 6 s Ar purge.

through the South West Academy of Nanoelecronics (SWAN), and Experiments were performed in the UCSD Nano3 facility supported by the NNCI (ECCS-1542148).

Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at https://doi.org/10.1016/j.apsusc.2018.08.034.

References

- [1] F. Schwierz, Graphene transistors, Nat. Nanotechnol. 5 (2010) 487–496.
- [2] H. Fang, S. Chuang, T.C. Chang, K. Takei, T. Takahashi, A. Javey, High-performance single layered WSe 2 p-FETs with chemically doped contacts, Nano Lett. 12 (2012) 3788–3792.
- [3] Y. Cui, R. Xin, Z. Yu, Y. Pan, Z.-Y. Ong, X. Wei, J. Wang, H. Nan, Z. Ni, Y. Wu, T. Chen, Y. Shi, B. Wang, G. Zhang, Y.-W. Zhang, X. Wang, High-performance monolayer WS ₂ field-effect transistors on high-κ dielectrics, Adv. Mater. 27 (2015) 5230–5234.
- [4] N.R. Pradhan, D. Rhodes, S. Feng, Y. Xin, S. Memaran, B.-H. Moon, H. Terrones, M. Terrones, L. Balicas, Field-effect transistors based on few-layered α-MoTe₂, ACS Nano 8 (2014) 5911–5920.

- [5] R. Ganatra, Q. Zhang, Few-layer MoS₂: a promising layered semiconductor, ACS Nano 8 (2014) 4074–4099.
- [6] S. Kim, A. Konar, W.-S. Hwang, J.H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y.W. Jin, S.Y. Lee, D. Jena, W. Choi, K. Kim, High-mobility and lowpower thin-film transistors based on multilayer MoS₂ crystals, Nat. Commun. 3 (2012) 1011.
- [7] B. Radisavljevic, A. Kis, Mobility engineering and a metal-insulator transition in monolayer MoS₂, Nat. Mater. 12 (2013) 815–820.
- [8] Q.H. Wang, K. Kalantar-Zadeh, A. Kis, J.N. Coleman, M.S. Strano, Electronics and optoelectronics of two-dimensional transition metal dichalcogenides, Nat. Nanotechnol. 7 (2012) 699–712.
- [9] S.Z. Butler, S.M. Hollen, L. Cao, Y. Cui, J.A. Gupta, H.R. Gutiérrez, T.F. Heinz, S.S. Hong, J. Huang, A.F. Ismach, E. Johnston-Halperin, M. Kuno, V.V. Plashnitsa, R.D. Robinson, R.S. Ruoff, S. Salahuddin, J. Shan, L. Shi, M.G. Spencer, M. Terrones, W. Windl, J.E. Goldberger, Progress, challenges, and opportunities in two-dimensional materials beyond graphene, ACS Nano 7 (2013) 2898–2926.
- [10] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S.K. Banerjee, L. Colombo, Electronics based on two-dimensional materials, Nat. Nanotechnol. 9 (2014) 768–779.
- [11] Y. Xuan, Y.Q. Wu, T. Shen, M. Qi, M.A. Capano, J.A. Cooper, P.D. Ye, Atomic-layerdeposited nanostructures for graphene-based nanoelectronics, Appl. Phys. Lett. 92 (2008) 13101.
- [12] A. Azcatl, S. McDonnell, K.C. Santhosh, X. Peng, H. Dong, X. Qin, R. Addou, G.I. Mordi, N. Lu, J. Kim, M.J. Kim, K. Cho, R.M. Wallace, MoS₂ functionalization for ultra-thin atomic layer deposited dielectrics, Appl. Phys. Lett. 104 (2014)

I. Kwak et al.

111601.

- [13] W. Yang, Q.-Q. Sun, Y. Geng, L. Chen, P. Zhou, S.-J. Ding, D.W. Zhang, The integration of sub-10 nm gate oxide on MoS₂ with ultra low leakage and enhanced mobility, Sci. Rep. 5 (2015) 11921.
- [14] M.J. Hollander, M. LaBella, Z.R. Hughes, M. Zhu, K.A. Trumbull, R. Cavalero, D.W. Snyder, X. Wang, E. Hwang, S. Datta, J.A. Robinson, Enhanced transport and transistor performance with oxide seeded high-κ gate dielectrics on wafer-scale epitaxial graphene, Nano Lett. 11 (2011) 3601–3607.
- [15] B. Fallahazad, K. Lee, G. Lian, S. Kim, C.M. Corbet, D.A. Ferrer, L. Colombo, E. Tutuc, Scaling of Al₂O₃ dielectric for graphene field-effect transistors, Appl. Phys. Lett. 100 (2012) 93112.
- [16] Surface modification of diamond-like carbon films to graphene under low energy ion beam irradiation, Appl. Surf. Sci., 258 (2012) 2931–2934.
- [17] B. Lee, S.-Y. Park, H.-C. Kim, K. Cho, E.M. Vogel, M.J. Kim, R.M. Wallace, J. Kim, Conformal Al₂O₃ dielectric layer deposited by atomic layer deposition for graphenebased nanoelectronics, Appl. Phys. Lett. 92 (2008) 203102.
- [18] A. Azcatl, K.C. Santhosh, X. Peng, N. Lu, S. McDonnell, X. Qin, F. de Dios, R. Addou, J. Kim, M.J. Kim, K. Cho, R.M. Wallace, HfO2 on UV–O3 exposed transition metal dichalcogenides: interfacial reactions study, 2D Mater. 2 (2015) 14004.
- [19] J. Yang, S. Kim, W. Choi, S.H. Park, Y. Jung, M.-H. Cho, H. Kim, Improved growth behavior of atomic-layer-deposited high-k dielectrics on Multilayer MoS₂ by oxygen plasma pretreatment, ACS Appl. Mater. Interfaces 5 (2013) 4739–4744.
- [20] Y. Oshima, M. Shandalov, Y. Sun, P. Pianetta, P.C. McIntyre, Hafnium oxide/germanium oxynitride gate stacks on germanium: capacitance scaling and interface state density, Appl. Phys. Lett. 94 (2009) 183102.
- [21] D.K. Schroder, Semiconductor Material and Device Characterization, IEEE Press, 2006.
- [22] G. Dingemans, M.C.M. van de Sanden, W.M.M. Kessels, Influence of the deposition temperature on the c-Si surface passivation by Al₂O₃ films synthesized by ALD and PECVD, Electrochem. Solid-State Lett. 13 (2010) H76.
- [23] H. Liu, K. Xu, X. Zhang, P.D. Ye, The integration of high-k dielectric on two-dimensional crystals by atomic layer deposition, Appl. Phys. Lett. 100 (2012) 152115.

- [24] B.R. Scharifker, J. Mostany, Three-dimensional nucleation with diffusion controlled growth: Part I. Number density of active sites and nucleation rates per site, J. Electroanal. Chem. Interfacial Electrochem. 177 (1984) 13–23.
- [25] M.D. Groner, F.H. Fabreguette, J.W. Elam, S.M. George, Low-temperature Al₂O₃ atomic layer deposition, Chem. Mater. 16 (2004) 639–645.
- [26] M.D. Groner, J.W. Elam, F.H. Fabreguette, S.M. George, Electrical characterization of thin Al2O3 films grown by atomic layer deposition on silicon and various metal substrates, Thin Solid Films. 413 (2002) 186–197.
- [27] M. Ebrish, Graphene Quantum Capacitance Varactors (2015).
- [28] J.H. Park, H.C.P. Movva, E. Chagarov, K. Sardashti, H. Chou, I. Kwak, K.-T. Hu, S.K. Fullerton-Shirey, P. Choudhury, S.K. Banerjee, A.C. Kummel, *In Situ* observation of initial stage in dielectric growth and deposition of ultrahigh nucleation density dielectric on two-dimensional surfaces, Nano Lett. 15 (2015) 6626–6633.
- [29] Y. Kim, S.M. Lee, C.S. Park, S.I. Lee, M.Y. Lee, Substrate dependence on the optical properties of Al₂O₃ films grown by atomic layer deposition, Appl. Phys. Lett. 71 (1997) 3604–3606.
- [30] L. Zhang, Y. Guo, V.V. Hassan, K. Tang, M.A. Foad, J.C. Woicik, P. Pianetta, J. Robertson, P.C. McIntyre, Interface engineering for atomic layer deposited alumina gate dielectric on SiGe substrates, ACS Appl. Mater. Interfaces 8 (2016) 19110–19118.
- [31] S. Fadida, P. Shekhter, D. Cvetko, L. Floreano, A. Verdini, L. Nyns, S. Van Elshocht, I. Kymissis, M. Eizenberg, Direct observation of both contact and remote oxygen scavenging of GeO 2 in a metal-oxide-semiconductor stack, J. Appl. Phys. 116 (2014) 164101.
- [32] H. Kim, P.C. McIntyre, C. On Chui, K.C. Saraswat, S. Stemmer, Engineering chemically abrupt high-k metal oxide/silicon interfaces using an oxygen-gettering metal overlayer, J. Appl. Phys. 96 (2004) 3467–3472.
- [33] C. Choi, J.C. Lee, Scaling equivalent oxide thickness with flat band voltage (VFB) modulation using *in situ* Ti and Hf interposed in a metal/high-k gate stack, J. Appl. Phys. 108 (2010) 64107.
- [34] X. Li, T. Yajima, T. Nishimura, A. Toriumi, Study of Si kinetics in interfacial SiO 2 scavenging in HfO 2 gate stacks, Appl. Phys. Exp. 8 (2015) 61304.