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Ultralow Defect Density at Sub-0.5 nm HfO_2/SiGe Interfaces via Selective Oxygen Scavenging

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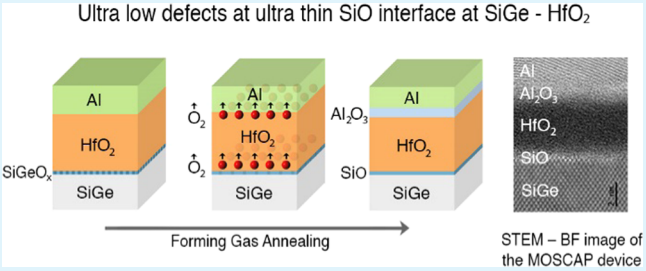
Supporting Information

ABSTRACT: The superior carrier mobility of SiGe alloys make them a highly desirable channel material in complementary metal-oxide-semiconductor (CMOS) transistors. Passivation of the SiGe surface and the associated minimization of interface defects between SiGe channels and high-k dielectrics continues to be a challenge for fabrication of high-performance SiGe CMOS. A primary source of interface defects is interfacial GeO_x. This interfacial oxide can be decomposed using an oxygen-scavenging reactive gate metal, which nearly eliminates the interfacial oxides, thereby decreasing the amount of GeO_x at the interface; the remaining ultrathin interlayer is consistent with a SiO_x-rich interface. Density functional theory simulations demonstrate that a sub-0.5 nm thick SiO_x-rich surface layer can produce an electrically passivated HfO_2/SiGe interface. To form this SiO_x-rich interlayer, metal gate stack designs including Al/HfO_2/SiGe and Pd/Ti/TiN/nanolaminate (NL)/SiGe (NL: HfO_2−Al_2O_3) were investigated. As compared to the control Ni-gated devices, those with Al/HfO_2/SiGe gate stacks demonstrated more than an order of magnitude reduction in interface defect density with a sub-0.5 nm SiO_x-rich interfacial layer. To further increase the oxide capacitance, the devices were fabricated with a Ti oxygen scavenging layer separated from the HfO_2 by a conductive TiN diffusion barrier (remote scavenging). The Pd/Ti/TiN/NL/SiGe structures exhibited significant capacitance enhancement along with a reduction in interface defect density.



KEYWORDS: *SiGe CMOS, high-mobility transistor, low-power electronics, high-k dielectric, interface traps, atomic layer deposition*

INTRODUCTION

Demand for low-power electronic devices drives research on high-mobility channel materials with high-k dielectric gate oxides for better electrostatic control of channels in transistors beyond the 14 nm node.[1] Complementary metal-oxide-semiconductor (CMOS) compatible SiGe[1,2] alloys are a potential Si replacement because of their higher mobility[3,4] and band gap tunability. However, integration of SiGe channels into CMOS is challenging in part because of defective interfacial oxide formation between SiGe and high-k dielectrics.[5] SiGe surface passivation is problematic due to the formation of mixed SiO_x−GeO_x interlayer oxides and the differences in thermal stability of the oxides of Si and Ge.[6] Suboxides of Ge are associated with defects at the high-k/SiGe interface,[7] GeO_2 is water soluble,[8] and GeO_x can diffuse into high-k dielectrics degrading device performance.[9,10] Recently, density functional theory (DFT) calculations by Chagarov et al.[11] showed that even though SiO_2 or GeO_x formation at the SiGe/HfO_2 interface induces trap states in the band gap before forming gas anneal (FGA) (passivation of Ge and Si dangling bonds by atomic hydrogen), a defect-free band gap can be established with monolayer Si−O termination of SiGe surfaces bonding to a HfO_2 high-k dielectric even before forming gas anneal. Preferential Si oxidation and selective Si−O formation on the SiGe surface is a challenging process during atomic layer deposition (ALD) due to excess oxygen-containing molecules in ALD reactors at elevated temperatures.[9,12] However, post-ALD processing may be employed to form very thin SiO_x-rich oxide/SiGe interfaces via an enthalpy-driven process of oxygen scavenging using a reactive gettering metal gate after ALD oxide deposition. In this approach, GeO_x can be selectively reduced to Ge, forming a SiO_x-rich

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interface[6,8] by utilizing the difference in heat of formation between GeO_2 ($\Delta H^{\circ}_{f,solid}$ = −580.0 kJ/mol), GeO ($\Delta H^{\circ}_{f,solid}$ = −261.9 kJ/mol), SiO ($\Delta H^{\circ}_{f,amorphous}$ = −423.42 kJ/mol),[13] and SiO_2 ($\Delta H^{\circ}_{f,solid}$ = −905.49 kJ/mol).[14] Oxygen scavenging by reactive metal gates is a well-known technique used for thinning low-k interfacial oxide layers in MOS gate stacks.[15,16] Previously, a reactive metal Ti gate was utilized to remove the interfacial layer (IL) between HfO_2 and Si, dissolving oxygen by Ti, which stayed metallic after the scavenging process.[15] Furthermore, oxygen scavenging using Al gates, due to this metal's high oxide formation enthalpy (Al_2O_3: $\Delta H^{\circ}_{f,solid}$ = −417.45 kJ/mol), was reported to induce GeO_x decomposition at a high-k/SiGe interface.[17] Selective oxygen scavenging from the GeO_x component of the IL in Al/Al_2O_3/$Si_{0.55}Ge_{45}$ gate stacks was observed, resulting in low interface defect density.[18]

Hafnium oxide is the preferred gate dielectric in CMOS due to the combination of high thermal stability, high permittivity, and sufficiently large band gap.[19] Oxygen scavenging from mixed Si−Ge oxide ILs at the HfO_2/SiGe interface will be distinct from those with Al_2O_3 gate oxides because HfO_2 is a relatively poor oxygen diffusion barrier compared to Al_2O_3.[20] In this paper, the impact of oxygen scavenging using Al in the gate metal structure of HfO_2/SiGe metal-oxide-semiconductor (MOS) gate stacks was investigated. The oxygen scavenging process was utilized to thin the interlayer and form a Si-rich interface. A successful selective scavenging process, which provides more than a 10× reduction in total interface trapped charge density (D_{it}) across the band gap with a very thin residual IL was demonstrated in Al-gated devices. In addition, remote oxygen scavenging with a reactive Ti gate in a Pd/Ti/TiN/nanolaminate (NL)/SiGe/Si structure was studied. In remote scavenging, the reactive gettering metal was separated from the HfO_2 by a conductive TiN diffusion barrier to form higher capacitance gate stacks. Results indicate effective interface defect reduction by remote oxygen gettering and enhanced gate capacitance in MOS capacitors with a Ti-containing metal gate structure due to IL thinning.

MATERIALS AND METHODS

As illustrated in Figure 1, the high-k/SiGe interface was studied with MOS capacitors (MOSCAPs) and fabricated on epitaxially grown, strained $Si_{0.7}Ge_{0.3}$ on p-type Si (100) (Applied Materials). Samples were degreased for 1 min by sonication in methanol and rinsed with acetone, isopropyl alcohol, and deionized (DI) H_2O. Before ALD oxide deposition, native oxides were removed by cyclic cleaning in HF (2%) and DI water 2.5 times for 1 min each half cycle ending with HF. After N_2 drying, the samples were dipped in ammonium sulfide solution (25% $(NH_4)_2S$) for 15 min for sulfur surface passivation.[21] After rinsing with DI water for 30 s and drying with N_2, the samples were transferred into the ALD system via a load lock with approximately 1 min of air exposure. High-k oxides were grown using a Beneq TFS200 cross flow, hot wall ALD reactor at 275 °C using $HfCl_4$ at 200 °C as the hot source precursor and $Al(CH_3)_3$ (trimethyl aluminum, TMA) at 25 °C. Both processes used water as the oxidant source. The HfO_2 deposition was carried out using 250 ms pulses of $HfCl_4$ with 500 ms pulses of H_2O, and the Al_2O_3 deposition was carried out using 1 s pulses of TMA followed by 500 ms pulses of H_2O. Growth rates for both processes were found to be ∼1 Å/cycle extracted from oxide thicknesses obtained from cross-sectional scanning transmission electron microscopy (STEM) images. Ar carrier gas at 2−3 Torr was used for all processes and a 6 s purge was employed between pulses.

Control samples with Ni gates and samples with reactive Al gates were deposited with a shadow mask (50 nm thick and 150 μm diameter) using a Denton 502A thermal evaporator in <2 × 10^{-6} Torr vacuum. Gettering gate stacks with Ti encapsulated between TiN and Pd (7/30/30 nm thick Pd/Ti/TiN) were sputtered using the same shadow mask at 5 mTorr without a vacuum break at a power of 200/200/100 W for 30/55/120 s (Pt/Ti/TiN), respectively, with a Denton Discovery 18 sputter system. The TiN acts as a diffusion barrier, and the Pd prevents ambient oxidation of the gate stack as well as promotes the dissociation of hydrogen during forming gas anneal. Native oxide was removed with 1 min of Ar plasma treatment and Al back contacts were subsequently sputtered in the same tool. The samples were annealed sequentially at 300, 330, and 350 °C for 10 min in forming gas (5% H_2, 95% N_2) in an Ulvac Mila-3000 minilamp annealing system; this was a carefully optimized procedure for Ni-gated nanolaminate MOSCAP devices. Capacitance−voltage (C−V) were recorded after each annealing step to determine the optimum annealing times at each temperature. Additional annealing at higher temperature, 400 °C, increased the defect density. It is noted that the annealing procedure was not optimized independently for each type of samples, but, instead, this optimized FGA for the Ni-gated nanolaminate MOSCAP was employed for all the samples. Electrical characterization of the MOSCAPs was performed using a Keysight B1500 at room temperature. Leakage currents (I_g − V_g) were measured from 2 to −2 V direct current gate bias and multifrequency capacitance−voltage (C−V) along with conductance−voltage (G−V) measurements were obtained from 10 kHz to 1 MHz in the same bias range. Following electrical characterization, cross-sectional TEM specimens (<100 nm) were prepared from MOSCAP devices using a FEI-Scios Ga focus ion beam. The structure and composition of the high-k/SiGe gate stacks were studied with high-resolution scanning transmission electron microscopy (HR-STEM) using a FEI Metrios TEM and a JEOL-ARM300F in the STEM mode operating at 200 kV. High-angle annular dark field (HAADF) and bright field (BF) mode was used for imaging. Electron energy loss spectroscopy (EELS) and energy-dispersive X-ray spectroscopy (EDS) were performed for local compositional analysis.

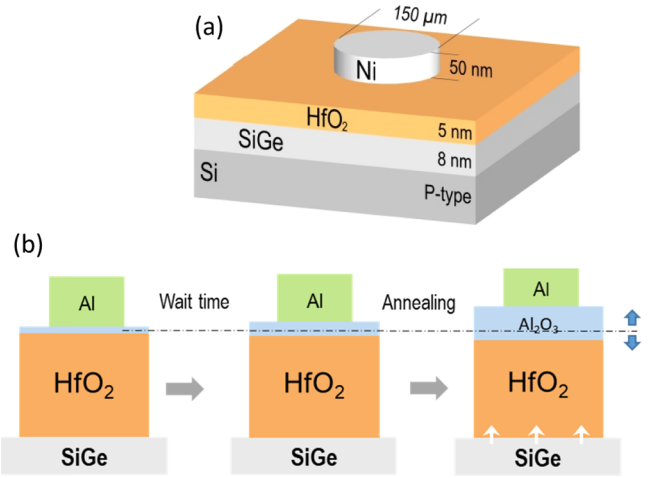

Figure 1. Schematic diagram of MOSCAP structure and gettering process. (a) Structure of the MOSCAP device. (b) Oxygen gettering process with an Al gettering gate. Al metal oxidizes with time and during forming gas anneal by the oxygen scavenged from interface as well as the excess of oxygen in HfO_2. White arrows denote scavenged oxygen from the interface during the anneal.

RESULTS AND DISCUSSION

Ni- and Al-gated HfO_2/SiGe/Si MOSCAPs with identical gate oxide deposition were compared with electrical measurements. Leakage currents for Ni-gated control devices (<2 × 10^{-4} A/cm^2) were found to be approximately 100× higher in comparison with the Al-gated devices (<2 × 10^{-6} A/cm^2) measured in accumulation at V_g = −1 V (Figure S1). Interface

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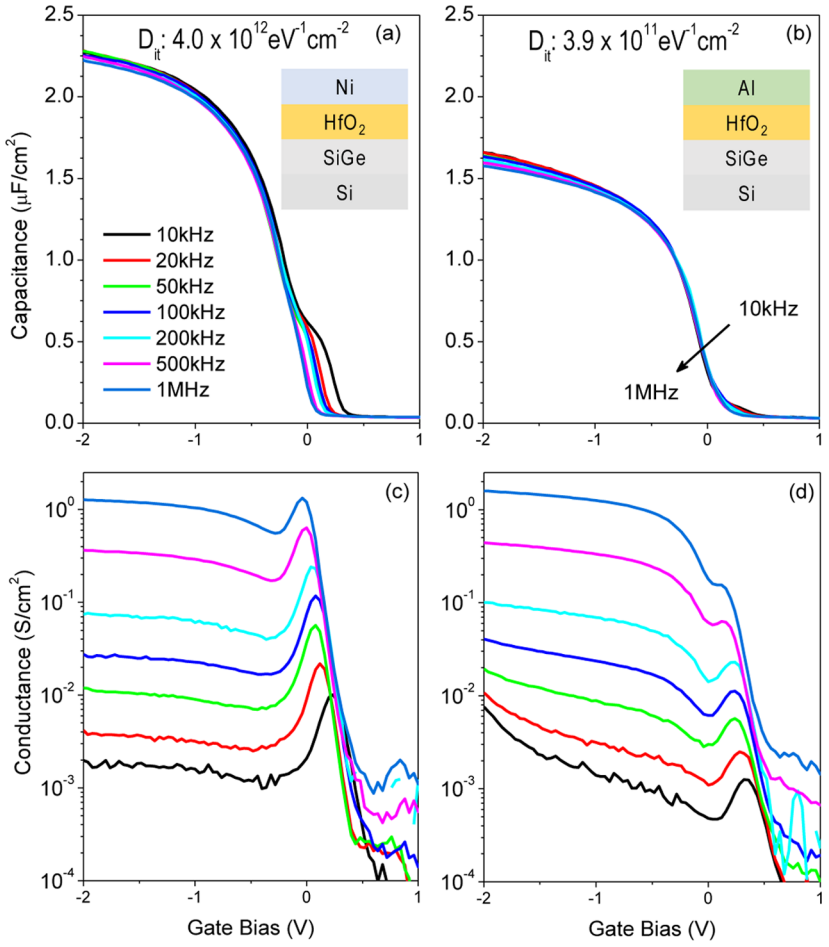

Figure 2. Defect characterization of Ni vs Al gates on HfO_2/SiGe MOSCAPs. Multifrequency $C-V$ (a, b) and $G-V$ (c, d) graphs of Ni- and Al-gated MOSCAPs from 10 kHz to 1 MHz. Insets illustrate the device structures. The Al-gated devices exhibit smaller D_{it} humps in the depletion region and lower peak conductance. Inset peak D_{it} values were calculated with the full interface state model and show a 10× reduction in defect density with reactive Al gates in comparison to Ni controls.

defects were characterized at room temperature with multifrequency $C-V$ and $G-V$ spectroscopy measurements performed at 10 kHz to 1 MHz from inversion of 2 V to accumulation of −2 V, and the results shown in Figure 2a−d indicates two notable differences between the Ni control and Al gates. (1) First, the depletion capacitance induced by defects at the high-k/SiGe interface has a much smaller D_{it} hump for Al gettering gate devices in comparison to Ni controls, indicating a better interface between HfO_2 and SiGe with Al gates. The depletion conductance also shows a lower peak value for the Al-gated device. The defect density was calculated from the maximum of G_p/ω versus ω using the conductance method[22] (Figure S2). Due to similar G_p/ω peak values for several bias points, defect density was further analyzed with the full interface state model[23] by fitting capacitance and conductance curves for each bias point as shown in Figure 3. The values extracted with both models are consistent and show maximum defect density close to the valence band; however, Al-gated devices have a lower defect density across entire band gap in comparison to Ni-gated devices. Peak defect densities of 4.0×10^{12} eV^{-1} cm^{-2} for Ni-gated and 3.9×10^{11} eV^{-1} cm^{-2} for Al-gated devices were observed at 0.25 and 0.36 eV above from valence band, respectively. Furthermore, the total integrated defect density was also found to be an order of magnitude lower for Al gates.

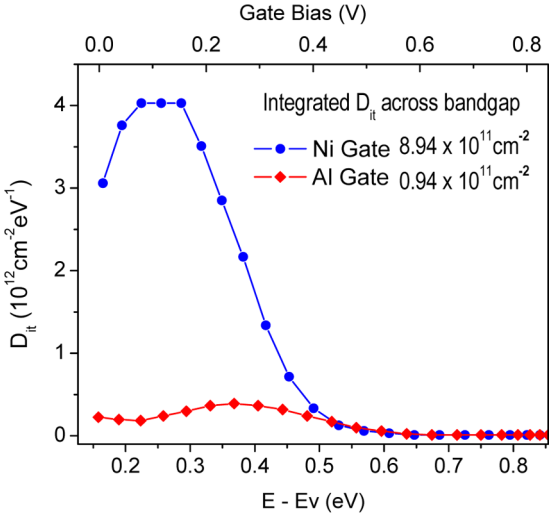

Figure 3. Interface defect density distributions for Al- and Ni-gated MOSCAP devices extracted with the full interface state model. In comparison with Ni controls, Al gettering gate devices show lower defect densities across the full energy range of the band gap. The integrated defect densities indicate a ∼10× reduction in total defect density across the band gap with Al-gated device.

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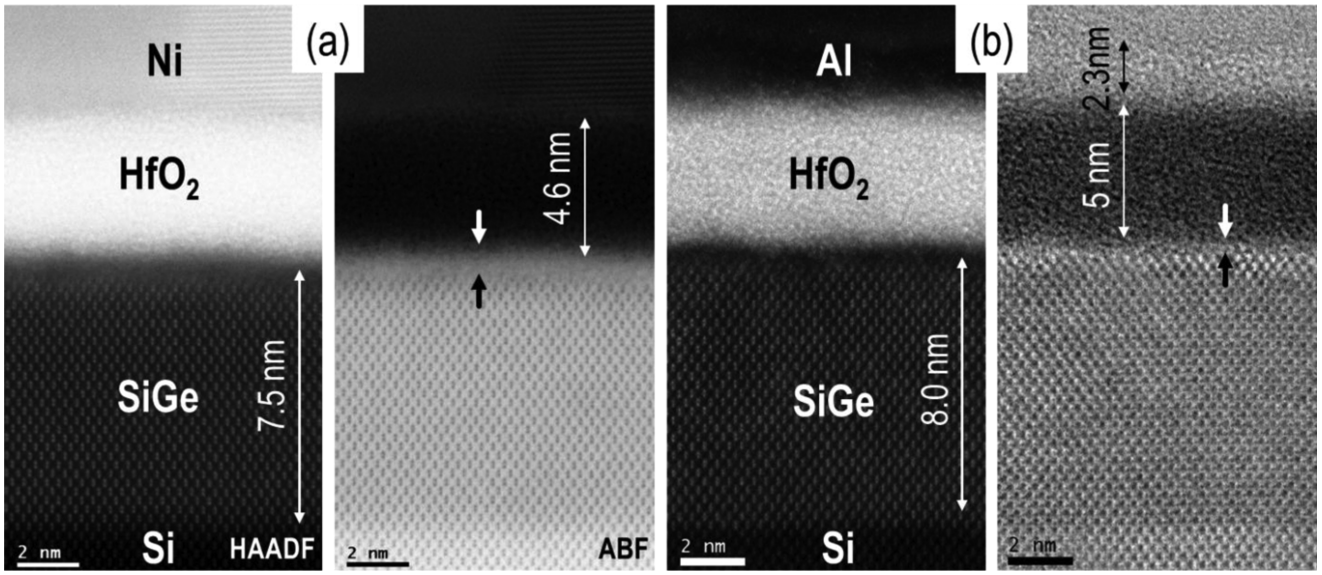

Figure 4. HR-STEM images of control Ni (a) and Al (b) gate HfO_2/SiGe MOSCAPs. In these images, oxide structures and regions defined according to contrast difference in which Ni-gated device displays two regions, gate oxide and IL, in contrast to Al, which has additional layer of 2.3 nm on gate oxide. In comparison to Ni control, the Al-gated device shows sub-0.5 nm interfacial oxide layer in various locations.

Both the conductance and full interface state models consistently indicate at least a 10× reduction in interface defect density between HfO_2/SiGe with Al gettering gates as compared to the Ni control gates. (2) The second difference between Ni control and Al gate samples is that the accumulation capacitance densities (C_{max}) differ: for Ni gates, C_{max} = 2.3 $\mu F/cm^2$, whereas for Al gates, C_{max} = 1.6 $\mu F/cm^2$. This difference can be attributed mainly to a thicker gate oxide being formed with Al gate metal because the Al is in direct contact with HfO_2 oxidizes to Al_2O_3 via oxygen scavenged from the interface and possibly from excess oxygen in the HfO_2[24] (Figures S3 and S4). In addition, Ge atoms decomposed from GeO_x on SiGe may possibly regrow on SiGe surface and contribute to the lower capacitance density as observed by Kim et al. for SiO_2 decomposition at HfO_2/Si interfaces.[15]

High-resolution scanning transmission electron microscopy (HR-STEM) high angle annular dark field (HAADF) and bright field (BF) images of the MOSCAPs shown in Figure 4 support the hypothesis of Al gates inducing formation of a thicker oxide: Al gates show a 2.7 nm thicker gate oxide as compared to the Ni-gated control. The bright field image in Figure 4b clearly indicates the formation of a second amorphous oxide layer in the Al gate region. The most significant difference between Ni- and Al-gated devices in the STEM images is the interface region where Al gates show a very thin interface layer compared to Ni-gated devices. In some locations, a few monolayers of oxide or even direct bonding of HfO_2 to the channel is apparent for the Al gates.

The low defect interface in Al-gated MOSCAPs was further investigated with compositional analysis by energy-dispersive X-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS) as shown in Figure 5. The elemental composition was traced to determine the positions and compositions of various interlayers. Black and green dashed lines intercept the half peak values of the Si and Ge elemental intensity profile and define the interface layer region. As indicated by the black and green arrows, the interface is Si-rich. This is consistent with low defect interface formation by GeO_x suppression. Very

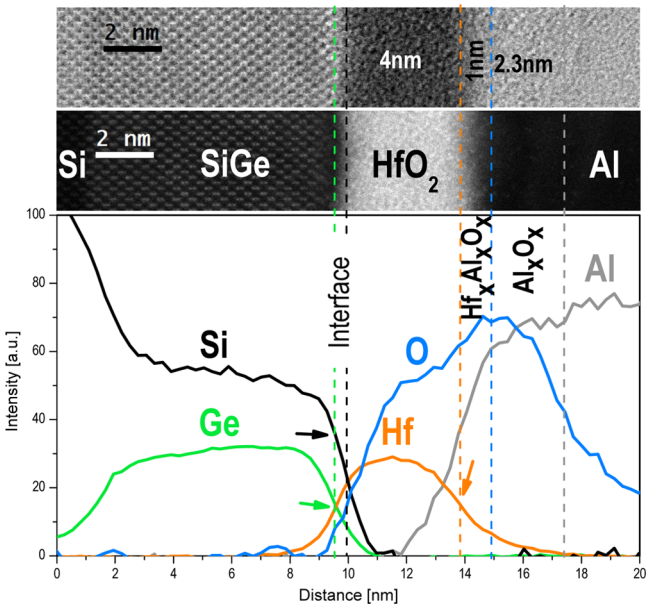

Figure 5. HR-STEM images and corresponding EELS compositional analysis of Al/HfO_2/SiGe/Si MOSCAP. In this STEM image, the regions of gate oxide are defined using compositions obtained with EELS spectra. In contrast to three regions defined in STEM image of Al/HfO_2/SiGe/Si in Figure 4, EELS revealed four regions in the Al/HfO_2/SiGe/Si stacks. Green and black dashed lines intercept the half peak values of the Si and Ge signals and delineate the SiGe−HfO_2 interface. Black and green arrows denote Si and Ge composition on SiGe surface in which a Si-rich interface composition is detected. The orange line intercepts the half max of the Hf signal. The Hf asymmetrically tails into the Al gate metal, indicating that Hf and Al intermix. The blue dashed line indicates the max peak of oxygen, which is shifted with respect to the Hf peak toward the Al gate. The Al peak tail extends into the gate oxide, consistent with Al oxidation. The gray dashed line separates the regions of oxidized Al and elemental Al metal.

similar results were obtained with EDS (Figure S5), which was performed simultaneously with EELS. The data are consistent

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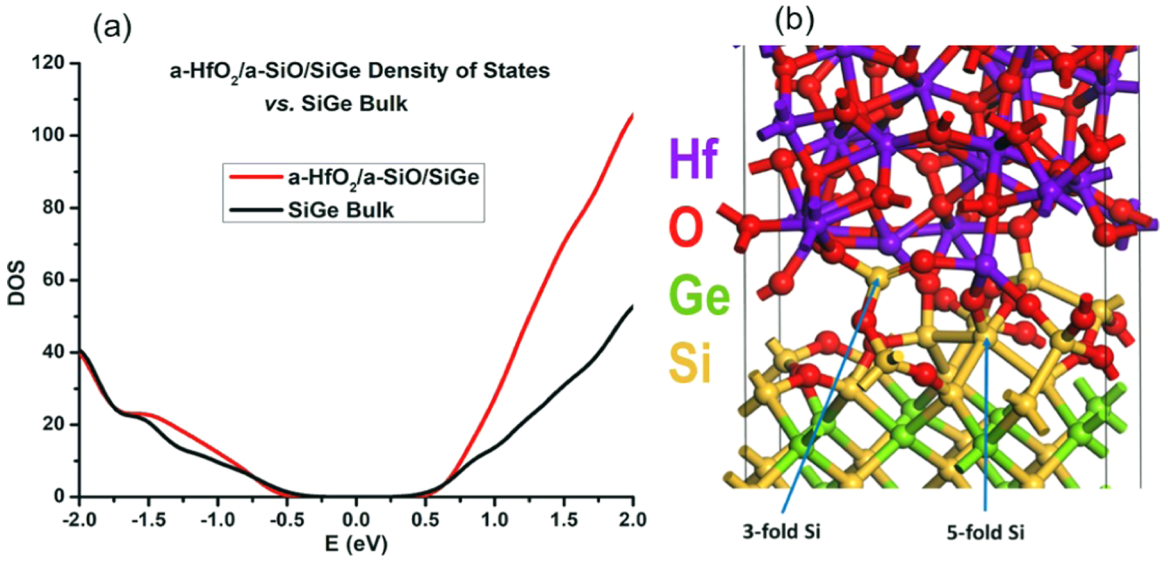

Figure 6. Density of states (a) and (b) interface bonding configuration for bulk SiGe and HfO_2/SiO/SiGe. DFT results for annealed and relaxed a-HfO_2/a-SiO/SiGe shows no energy states in band gap very similar to bulk SiGe. Corresponding interface structures illustrates 3-fold Si and 5-fold Si along with 4-fold Si bonding. Note the interfacial Si bonded to O, which is in nonstandard coordination, consistent with ionic bonding.

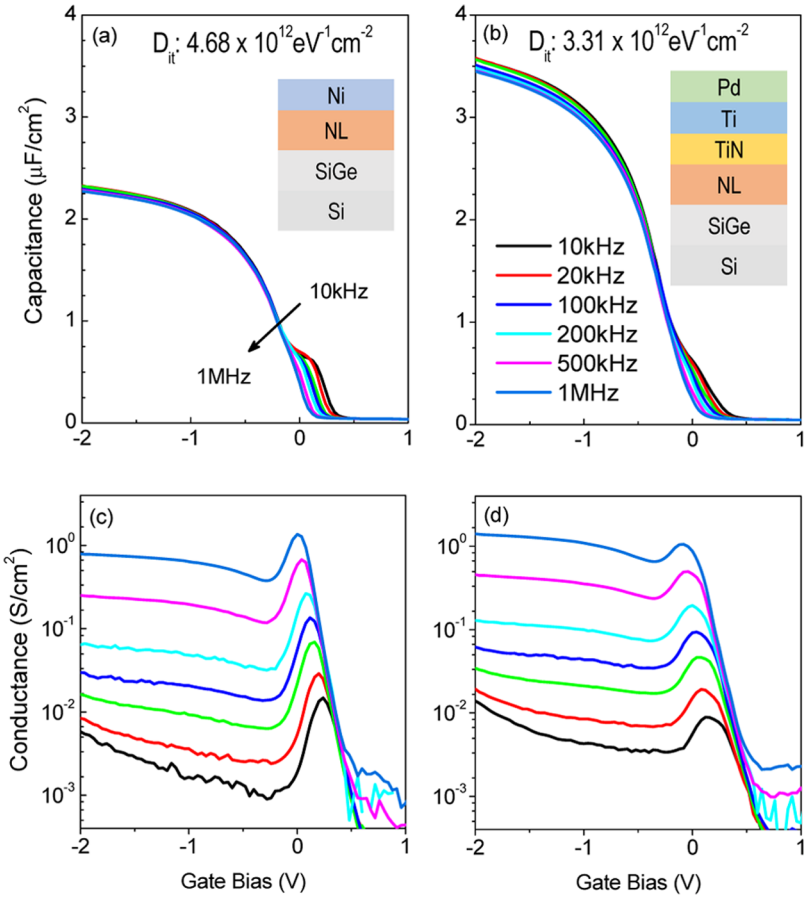

Figure 7. Multifrequency $C-V$ and $G-V$ spectroscopy of Ni and Ti gate MOSCAPs. (a, b) $C-V$ and (c, d) $G-V$ plots (10 kHz to 1 MHz) from accumulation −2 V to depletion 1 V for gettering Pd/Ti/TiN gates and Ni control MOS capacitors. Inset schematics illustrate the device structures. Peak D_{it} values in the band gap are shown. In comparison with Ni gates, Ti-gated MOSCAP show a lower D_{it} hump and corresponding lower conductance peak. Inset peak D_{it} values were obtained from the full interface state model. Ti-gated devices show a higher accumulation capacitance of 3.5 $\mu F/cm^2$, 40% higher than Ni-gated devices.

with the formation of a 1−2 monolayer-thick Si-rich interface oxide for the Al-gated HfO_2/SiGe MOSCAPs that exhibits very low D_{it}. The gate stack is found to have four oxide regions: Al_2O_3, $Al_xHf_xO_x$, HfO_2, and SiO_x (IL). With respect to the Hf peak, the oxygen peak is shifted toward the Al gate. The Al signal tail extends into gate oxide, indicating Al oxidation at the

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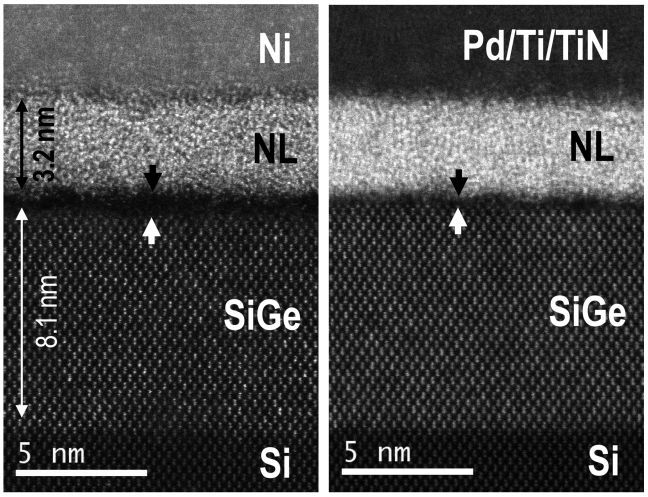
HfO_2/Al gate interface. The orange dashed line intercepts the half peak of Hf and the tail of the Hf extends into Al. This is consistent with interdiffusion forming a $Hf_xAl_xO_x$ region, although interface roughness will also contribute to apparent intermixing. Extension of the oxygen tail into the Al gate beyond the Hf peak is consistent with Al_xO_y formation. This thicker gate oxide formed by local Al oxidation is consistent with the 100× lower leakage and 0.7 $\mu F/cm^2$ reduction in C_{max} observed in $I-V$ and $C-V$ measurements (see the Supporting Information). The data are consistent with the Al gate either decomposing GeO_x at the interface or removing GeO from the interface via oxygen scavenging[18] to form an SiO_x-rich interface and an order of magnitude reduction in interface defect density.

Formation of an interface with low defect density and SiO_x composition was studied with density functional theory (DFT). All the DFT simulations were performed with the Vienna ab initio simulation package using projector augmented-wave pseudopotentials and the Perdew–Burke–Ernzerhof exchange–correlation functional.[25] The a-HfO_2 sample was stoichiometric and included 40 Hf and 80 O atoms. Several a-HfO_2 samples were generated using hybrid classical and DFT-molecular dynamics simulations including annealing, cooling, and relaxation. The amorphous sample quality was verified via radial-distribution function main peak positions, average nearest neighbor numbers, nearest neighbor distributions, and DFT-calculated[26] band gaps demonstrating good correlation to the available simulated and experimental reference properties.[27] The sample with the best match to experimental data was selected and used for simulations. The amorphous samples were generated to match the SiGe(001) surface area. A more detailed explanation of a-HfO_2 sample generation was presented elsewhere.[26] The density of states versus energy shown in Figure 6a indicates a defect-free band gap for the near-interface region of the SiGe channel, very similar to a SiGe bulk crystal. Figure 6b shows the corresponding bonding coordination of an interfacial a-SiO layer. In the simulation cell, there are two 3- and 5-fold coordinated interfacial Si atoms along with 4-fold interfacial Si, which do not create any mid-gap or band-edge states. These 3- and 5-fold coordinated Si atoms have multiple bonds to oxygen, which is consistent with the interfacial Si atoms having primarily ionic bonding, so a range of coordination can be tolerated.

Direct selective oxygen scavenging with Al metal gates causes an undesired reduction in C_{max} via the formation of a lower-k aluminum oxide layer in series with the HfO_2 gate dielectric. Remote oxygen scavenging with Ti gates encapsulated between TiN and Pd was investigated to prevent this unwanted capacitance reduction[15] (denoted as a Pd/Ti/TiN gate structure). Because Al_2O_3 is known to be a good diffusion barrier for Ge out diffusion,[20,28] Al_2O_3–HfO_2 nanolaminate oxide structures were chosen for this study and grown with four super cycles consisting of nine cycles of HfO_2 and one cycle of Al_2O_3. Pd/Ti/TiN gettering gate metal was also tested on only HfO_2 gate oxide, and a similar gettering process was observed. However, the nanolaminate structure was preferred for further compositional analysis due to the improved diffusion barriers formed with the nanolaminate, which prevents Ge out diffusion and provides lower leakage. Ge out diffusion into the gate oxide might induce reliability issues for device operation; therefore, nanolaminate HfO_2–Al_2O_3 structures were employed to prevent GeO_x diffusion to the gate metal. Similar leakage current density of 1.3×10^{-6} and 3.5×10^{-6} A/cm^2 at −1 V were obtained for Ni- and Pd/Ti/TiN-gated NL/SiGe/Si devices, respectively (Figure S1). Multifrequency $C-V$ and $G-V$ measurements are presented in Figure 7a–d. Comparison of the $C-V$ curves shows two notable differences between the Ni-gated control capacitors and the MOSCAPS with Pd/Ti/TiN gates. First, C_{max} is 3.5 $\mu F/cm^2$ for the oxygen-scavenging gates versus 2.25 $\mu F/cm^2$ for the Ni-gated controls. This significant increase in capacitance can be attributed to IL thinning with oxygen scavenging by the reactive Ti gates, as shown in the STEM images in Figure 8. The Ni-gated sample shows a ∼1.1 nm



Gate	Avg. high-k	Avg. IL	Avg. HK + IL
TiN/Ti/Pd	34.0Å	6.9Å	40.9Å
Ni	32.0Å	10.9Å	42.9Å

Figure 8. TEM analysis of interface thickness. HAADF images of Ni- and Pd/Ti/TiN-gated MOSCAP devices and table for average thickness of ILs and HfO_2–Al_2O_3 nanolaminate (NL) gate oxide. Ti-gated device shows thinner IL in comparison with the Ni control.

thick IL, whereas the sample with the Ti gate has 0.7 nm thick IL (Figure S6). However, the expected C_{max} value according to the TEM-derived oxide thicknesses is 2.8 $\mu F/cm^2$ instead of 3.5 $\mu F/cm^2$ for the Pd/Ti/TiN-gated MOSCAP (Figures S7 and S8). In this calculation, it is assumed that both devices have oxides with the same dielectric constant because they were grown simultaneously in the ALD reactor. Second, it is assumed that the dielectric constant of the IL formed at SiGe/HfO_2 is k = 4.5 as the IL consists of both SiO_2 (k = 3.9) and GeO_2 (k = 5.2).[29] Therefore, the C_{max} difference between the experimental and expected value for the Pd/Ti/TiN sample suggests permittivity modulation of the HfO_2, which is discussed in the Supporting Information. The equivalent oxide thickness (EOTs) for Ni-gated samples was found to be ∼1.5 nm, whereas Ti oxygen-scavenging gates have a notably lower EOT of ∼1 nm (Figure S9).

The second significant difference in the $C-V$ curves comparing the Ni- and Pd/Ti/TiN-gated samples is the hump in the depletion capacitance induced by defects at the high-k/SiGe interface, as shown in Figure 7. In comparison with the Ni-gated devices, Pd/Ti/TiN-gated devices have a smaller D_{it} hump, indicating a better interface between HfO_2 and SiGe with Pd/Ti/TiN vs Ni gates. Peak D_{it} of 3.31×10^{12}

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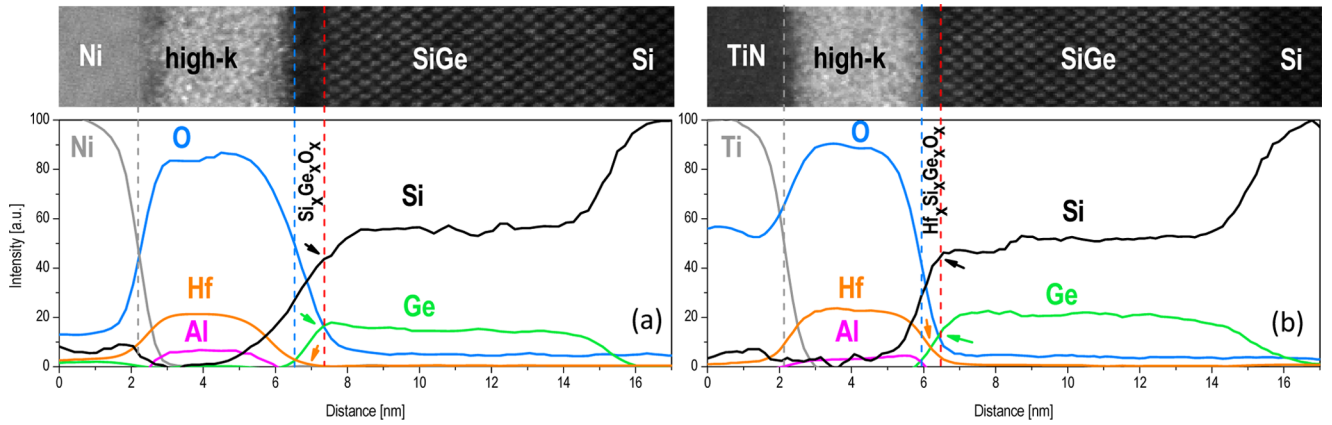

Figure 9. HAADF images and corresponding EELS analysis of (a) Ni/HfO_2−Al_2O_3-NL- and (b) Pd/Ti/TiN/HfO_2−Al_2O_3-NL-gated devices. The blue line intercepts the half max of the oxygen signal. The red line marks the SiGe surface atoms determined from the last row of crystallographically ordered atoms in the corresponding STEM image. Black and green arrows point to the Si and Ge composition at the SiGe surface. The orange arrow indicates the Hf compositions in the ILs. Ti-gated devices have a thinner Si-rich IL of ∼6 Å in comparison with ∼9 Å for the control Ni-gated devices. The Ti-gated devices also have a lower Ge content in the IL than Ni-gated devices; the Si/Ge ratio at the point of the red lines is 2.6 for the Ni-gated sample and 3.5 for the Ti-gated sample.

eV^{-1} cm^{-2} for Pd/Ti/TiN gates and 4.68×10^{12} eV^{-1} cm^{-2} for Ni were calculated according to the full interface state model[30] and similar values were obtained with the conductance method (Figure S10.). The defect distributions across the band gap calculated using the full interface state model (Figure S11) indicate less charge trap formation with Pd/Ti/TiN gates in comparison to Ni gates. Both the conductance and full interface state models show ∼30% reduction in D_{it} consistent with the formation of a higher quality interface between HfO_2 and SiGe.

Figure 9 shows the EELS analysis for the Ni/HfO_2−Al_2O_3-NL and Pd/Ti/TiN/HfO_2−Al_2O_3-NL samples. In comparison to the Ni/HfO_2−Al_2O_3-NL sample, the Pd/Ti/TiN/HfO_2−Al_2O_3-NL sample has an abrupt Si profile in the IL region. This may be the result of local variability of the interfaces. Another reason would be expected excess of oxygen in the HfO_2−Al_2O_3-NL for Ni/HfO_2−Al_2O_3-NL devices than for Pd/Ti/TiN/HfO_2−Al_2O_3-NL devices; it is hypothesized that the excess oxygen enhances Si diffusion into the HfO_2. The most important difference between these samples is the IL; a thinner IL is observed for Pd/Ti/TiN than for Ni gates. Furthermore, EELS analysis indicates a slightly lower Ge/Si ratio in the ILs for Pd/Ti/TiN- (0.32) vs Ni-gated (0.38) devices as indicated with green arrows. This difference correlates with the lower defect density obtained in the C−V analysis and indicates a successful GeO_x defect reduction with Ti gettering gates via remote oxygen scavenging through the TiN layer. The formation of SiO_x-rich interfaces with Ti gettering gates is consistent with the more favorable thermodynamics of Ge−O to Ti ligand exchange than Si−O to Ti−O ligand exchange. The excess interlayer Ge in Pd/Ti/TiN-gated device might have been evaporated in the form of GeO_x, or it may have regrown on SiGe epitaxially; however, the amount of Ge being regrown would be difficult to detect by TEM-EELS because the interlayers are less than 1 nm. GeO_x diffusion through gate oxides has been detected by XPS,[21] but again, the amount would be too small to detect by TEM-EELS. It is noted that in comparison to the Al gettering gate in Figure 2b, the Pd/Ti/TiN gettering gate in Figure 7b is less effective for interface defect reduction. It is hypothesized that this difference has multiple causes. First, TiN is known to be good diffusion barrier for oxygen, and this likely reduces the efficiency of the scavenging process. Second, the Ni gate is grown with thermal evaporation (a soft process); conversely, the Pd/Ti/TiN gate is grown by sputter deposition, which has energetic atoms and ions that can damage the oxide and the semiconductor interface. This sputter deposition induces additional defects at the interface of Pd/Ti/TiN gate, which results in a higher D_{it} before FGA (see Figure S13), which is partially recovered during FGA, but the damage recovery is not complete. Third, the FGA annealing was optimized for Ni-gated nanolaminate structure; therefore, further FGA optimization might be required for each device structure to improve the effectiveness of the scavenging process.

CONCLUSIONS

Oxygen-reactive Al and Pd/Ti/TiN gates were employed to reduce interface defects by scavenging oxygen from the SiGe/HfO_2 interface. In comparison with control Ni-gated devices, thinner IL formation in both Al and Pd/Ti/TiN-gated MOSCAPs were demonstrated using STEM. Lower interface defect formation with Al and Pd/Ti/TiN gettering gates coincided with a Si-rich interlayer formation as shown by STEM-EELS-EDS analysis. These results suggest that Al and Pd/Ti/TiN gates scavenge oxygen from the IL, forming a thinner interlayer that contains less GeO_x. By having less GeO_x at the interface, this process reduces interface defects. Whereas Al-gated devices exhibited a C_{max} reduction due to the formation of Al_2O_3 in contact with HfO_2, the Pd/Ti/TiN-gated device exhibited a C_{max} enhancement, as the oxidized metal layer (TiO_x) was separated from HfO_2 by a conductive diffusion barrier. Stable defect-free interface formation with a few monolayers of SiO on SiGe was demonstrated with DFT simulations.[26] The extremely thin interface with ultralow defect densities between SiGe/HfO_2 proves that a thick IL is not necessary.

ASSOCIATED CONTENT

Supporting Information

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Interface defect density calculation according to conductance and full interface state model, electron dispersion spectroscopy (EDS) analysis of Al/HfO_2/SiGe device, leakage characteristic of the devices presented in this study, calculation of C_{max} according to oxide thickness obtained from STEM, $C-V$ graph of devices before forming gas annealing (DOCX)

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Notes

The authors declare no competing financial interest.

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