ACSNANO
www.acsnano.org
ARTICLE

Atomic Layer Deposition of Al_2O_3 on WSe_2 Functionalized by Titanyl Phthalocyanine

Jun Hong Park,[†,¶] Sara Fathipour,[*,§,¶] Iljo Kwak,[†] Kasra Sardashti,[†] Christopher F. Ahles,[†] Steven F. Wolf,[†] Mary Edmonds,[†] Suresh Vishwanath,[§,∥] Huili Grace Xing,[§,∥,⊥] Susan K. Fullerton-Shirey,[#] Alan Seabaugh,[*,§] and Andrew C. Kummel[*,†,‡]

[†]Materials Science and Engineering Program and [‡]Departments of Chemistry and Biochemistry, University of California, San Diego, La Jolla, California 92093, United States

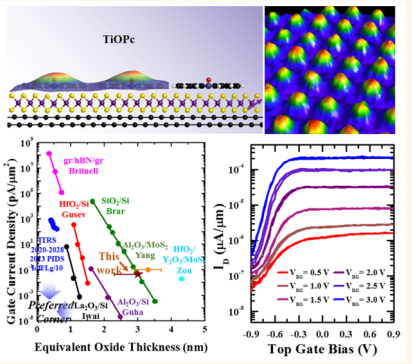
[§]Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556, United States

[∥]School of Electrical and Computer Engineering and [⊥]Department of Materials Science and Engineering, Cornell University, Ithaca, New York 14850, United States

[#]Department of Chemical and Petroleum Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania 15213, United States

Supporting Information

ABSTRACT: **To deposit an ultrathin dielectric onto WSe_2, monolayer titanyl phthalocyanine (TiOPc) is deposited by molecular beam epitaxy as a seed layer for atomic layer deposition (ALD) of Al_2O_3 on WSe_2. TiOPc molecules are arranged in a flat monolayer with 4-fold symmetry as measured by scanning tunneling microscopy. ALD pulses of trimethyl aluminum and H_2O nucleate on the TiOPc, resulting in a uniform deposition of Al_2O_3, as confirmed by atomic force microscopy and cross-sectional transmission electron microscopy. The field-effect transistors (FETs) formed using this process have a leakage current of 0.046 pA/μm^2 at 1 V gate bias with 3.0 nm equivalent oxide thickness, which is a lower leakage current than prior reports. The n-branch of the FET yielded a subthreshold swing of 80 mV/decade.**



KEYWORDS: *ALD, Al_2O_3, WSe_2, TiOPc, device*

For decades the semiconductor industry has continuously scaled the channel dimensions of complementary metal−oxide−semiconductor (CMOS) field-effect transistors (FET) to increase the packing density and boost performance.[1] However, as transistor dimensions have decreased to a few nanometers, CMOS technology has faced short channel effects and rising leakage current in the off state, resulting in large power consumption.[1,2] Previous experimental and theoretical research has suggested employing ultrathin channel bodies or large band gap materials to suppress short channel effects[3−5] and enhance the gate control.[6]

Two-dimensional (2D) materials, such as WSe_2, are being explored for transistors[7,8] and optoelectronic devices.[9,10] WSe_2 has an electron (hole) effective mass of 0.34 (0.44)[11] and ambipolar behavior in transistors.[12] Field-effect mobility for p-channel (n-channel) FETs has been reported as 202−250 $cm^2/(V\ s)$ for monolayer WSe_2.[12,13] In multilayer FETs, a wider range of mobilities has been reported: 500 $cm^2/(V\ s)$ for p-channel[14] and 70 $cm^2/(V\ s)$ for n-channel.[15] While the electrical properties of layered WSe_2 are promising, one challenge is the direct deposition of gate dielectrics due to the absence of surface dangling bonds. In contrast, successful methods of direct gate oxide atomic layer deposition (ALD) are now being reported on layered MoS_2.[16−19] For example, on MoS_2, Liu and Azcatl report that it is only necessary to reduce the temperature to 473 K during ALD deposition to achieve a uniform Al_2O_3 thickness of ∼10 nm.[16,17] Replacing the water pulse with ozone is also effective for nucleating Al_2O_3 on MoS_2 at 473 K.[18] More recently, remote O_2 plasma was demonstrated for seeding Al_2O_3 on MoS_2, again at 473 K.[19] However, for the deposition of dielectric on WSe_2, Azcatl and co-workers report that the ozone pretreatment on WSe_2 yielded islands of Al_2O_3 and possible interfacial reactions, so the approaches reported to date do not appear to translate across TMD materials.[20]

In this study, dielectrics with low leakage and low equivalent oxide thickness are demonstrated on WSe_2 using a titanyl phthalocyanine (TiOPc) monolayer (ML) as a seeding layer to nucleate ALD growth. Previously, the TiOPc seeding layer was integrated into graphene to deposit Al_2O_3 uniformly.[21] The density functional theory (DFT) calculations show a high

Received: April 20, 2016
Accepted: June 15, 2016

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX−XXX

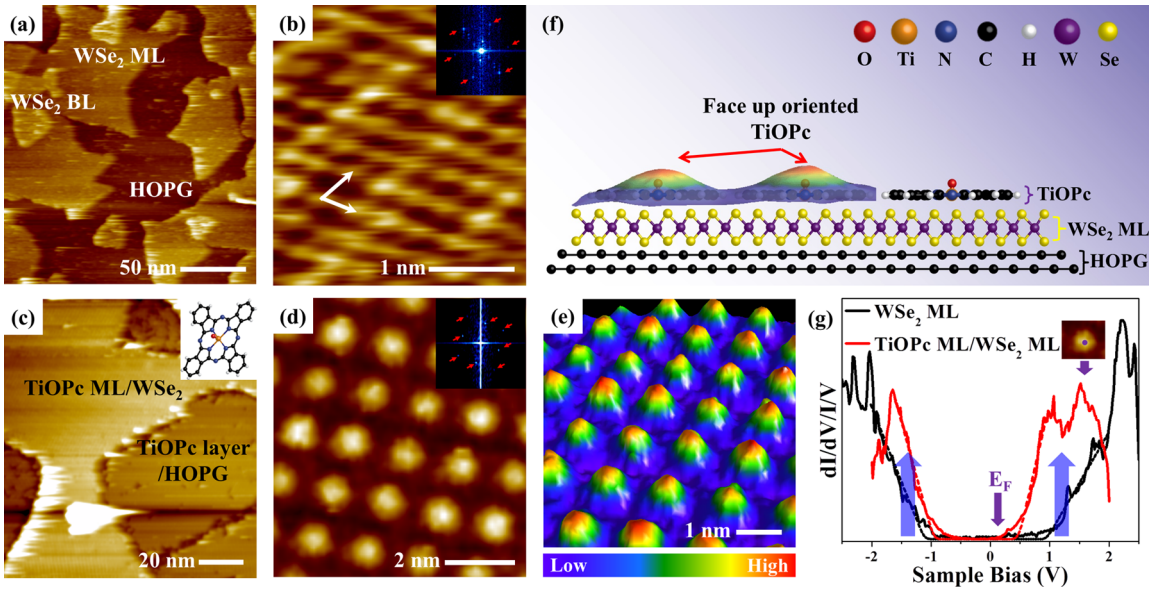


Figure 1. STM images of bare WSe_2/HOPG and monolayer TiOPc on WSe_2/HOPG. STM images recorded at 100 K. (a) Bare MBE-deposited WSe_2 layer on HOPG (V_S = 2.0 V, I_T = 30 pA). (b) Expanded STM image of WSe_2 with atomic resolution. Hexagonal atomic array of the Se topmost layer in WSe_2 (V_S = −2.0 V, I_T = 130 pA). The inset shows the Fourier transform of the atomic array of Se. (c) TiOPc ML deposited onto a WSe_2 ML on HOPG. The inset shows the molecular structure of TiOPc (V_S = 2.0 V, I_T = 20 pA). (d) Submolecular resolution of MBE TiOPc ML/WSe_2 ML/HOPG. The central O is observed as a bright spot (V_S = +2.0 V, I_T = 40 pA). The inset shows the Fourier transform of the TiOPc ML. (e) Three-dimensional STM image of the TiOPc ML with molecular resolution. (f) STM image of TiOPc molecules and schematic of the TiOPc ML, including the WSe_2 ML and the HOPG. The two TiOPc molecules on the left are overlapped with the STM image. (g) $(dI/dV)/(I/V)$ spectrum of bare WSe_2ML/HOPG and TiOPc ML/WSe_2 ML/HOPG.

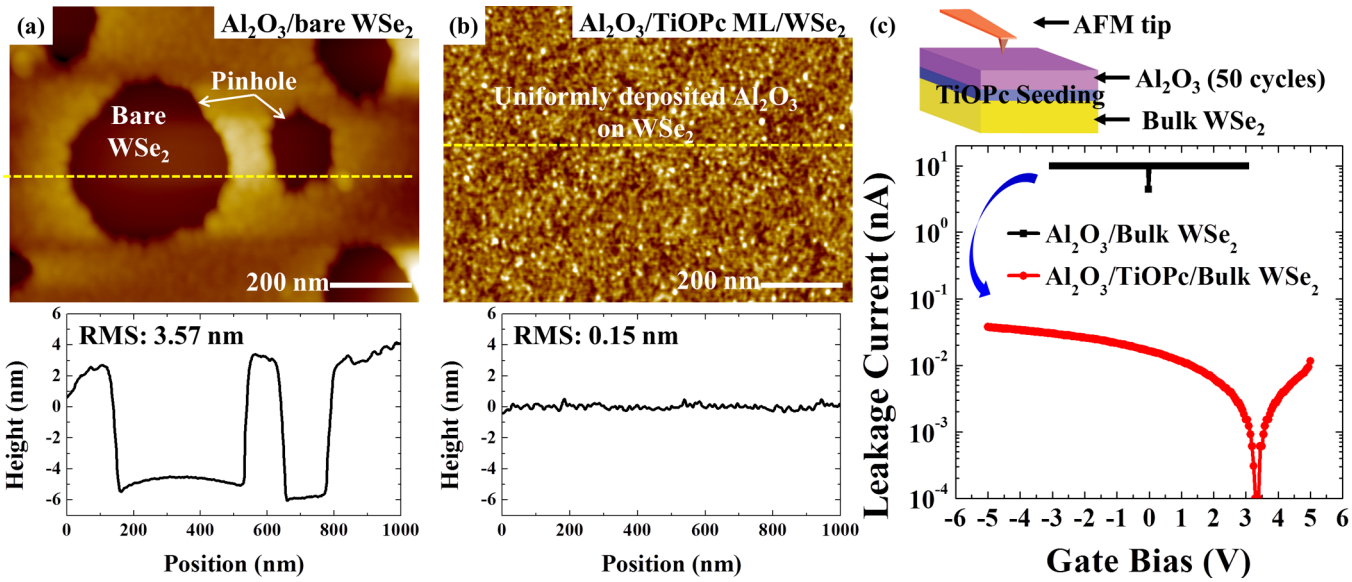


Figure 2. Topographic and electronic characteristics of Al_2O_3/TiOPc stack on bulk WSe_2 using AFM and C-AFM. (a) AFM image and corresponding line trace of Al_2O_3/bulk WSe_2 without the TiOPc layer. Pinholes that are about 5.5 nm deep are detected. (b) AFM image and line trace of Al_2O_3/TiOPc/bulk WSe_2. ALD dielectric is deposited uniformly on TiOPc/bulk WSe_2 with 0.15 nm RMS roughness. (c) C-AFM measurements of Al_2O_3 leakage currents prior to postdeposition anneal measured by C-AFM.

binding energy of dimethylaluminum, exceeding 1.5 eV with binding to the O, N, and C sites in TiOPc/graphene; thereby the uniformly deposited Al_2O_3 was obtained on graphene, as well as the over 1000 nF/cm^2 maximum capacitance in graphene capacitors. Similarly, using the TiOPc seeding layer, a uniformly deposited Al_2O_3 layer was obtained on multilayer WSe_2; then top-gated FETs were fabricated onto Al_2O_3/TiOPc/WSe_2 to evaluate the electrical property of the deposited dielectric and the FET. The deposited Al_2O_3 described here has a 3.0 equivalent oxide thickness (EOT) and 0.046 pA/μm^2 at 1 V, which is a lower leakage current than previously reported gate oxides on transition metal dichalcogenides (TMDs),[16,19] resulting in an 80 mV/dec subthreshold swing.

RESULTS AND DISCUSSION

Process Development on Epitaxial WSe_2. To develop the process, WSe_2 layers were first deposited on highly ordered

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX−XXX

pyrolytic graphite (HOPG) by molecular beam epitaxy (MBE). Scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) measurements of the MBE WSe_2 on HOPG are shown in Figure 1. The coexistence of ML and bilayer (BL) WSe_2 on HOPG and bare HOPG is shown in Figure 1a. The deposited WSe_2 ML has heights of about 0.7 nm (the line trace provided in Figure S1 of the Supporting Information), consistent with the three atomic layers' thickness (Se−W−Se) and prior AFM characterization of exfoliated single-layer WSe_2 flakes by Fang.[12] An atomically resolved filled-state STM image of ML WSe_2 (Figure 1b) shows the honeycomb atomic lattice of the topmost Se layer. There are no noticeable point defects or dislocations present. As shown in the STM image, the lattice parameter of WSe_2 is 0.32 ± 0.01 nm (standard error), which agrees with previous crystallography data, reporting 0.328 nm.[22] The Fourier transforms of the images in Figure 1b are shown as insets, confirming the hexagonal symmetry of the film; although the image is distorted due to thermal drift during the STM imaging, six distinct peaks are observed forming the hexagon shape (red arrows).

A ML of TiOPc was deposited on the MBE-grown WSe_2 on HOPG, and the empty-state STM image in Figure 1c shows a defect-free and highly ordered layer. The TiOPc molecular structure is shown in the inset of Figure 1c.[23] No domain boundaries, large-scale defects, or second-layer growth of TiOPc is observed, indicating a flat-lying and single-crystalline order in the TiOPc ML. As shown in the molecularly resolved STM image of Figure 1d, the O atom is located on top of the central Ti atom; the polarity of the TiOPc molecule arises from binding of this O with the central Ti. The STM image of TiOPc in Figure 1d is slightly distorted by the thermal drift during STM imaging; however, a square lattice of TiOPc molecules is clearly observed. This single-crystalline square lattice is confirmed by the Fourier transform, shown in the inset of Figure 1d, where 4-fold symmetry indicated by nine distinct peaks is observed. The 4-fold crystalline structure of the TiOPc ML on WSe_2/HOPG is clearly distinguished from the honeycomb lattice structure of WSe_2 on HOPG. It is noted that in the present observation the desorption temperature of a TiOPc ML on WSe_2 (523 K) in the UHV chamber is lower than the desorption temperature of a TiOPc ML on HOPG (623 K); annealing of TiOPc/WSe_2 above 523 K results in the degradation of the TiOPc crystal structure (see the Supporting Information, Figure 2S). Therefore, it follows that the TiOPc ML has a weaker van der Waals interaction with WSe_2 than with HOPG.[21]

A three-dimensionally rendered empty-state STM image of the ordered TiOPc ML is shown in Figure 1e. Each molecule shows a single bright peak, presumably from the center ring, while the outer aromatic rings show no significant features. This suggests that the highest tunneling currents occur at the titanyl group on the TiOPc molecules. The large electron collection at the center of the TiOPc can be interpreted as the titanyl up orientation as shown in Figure 1f, similar to the TiOPc ML on HOPG.[21] Consequently, the central O, which is charged negatively, faces the vacuum,[23−25] thereby providing potential binding sites for polar ALD precursors.

STS measurements of WSe_2/HOPG with and without TiOPc are used to determine how the surface electronic structure is changed upon TiOPc deposition, as shown in Figure 1g. The STS spectra on the TiOPc ML were recorded at the center of the molecules, as shown in the inset STM image in Figure 1g. The STS spectra show that the bare WSe_2/HOPG band gap is 2.05 ± 0.04 eV, and the Fermi level is positioned near the center of the band gap. The Fermi level is marked by the purple arrow at 0 V. TiOPc increases the density of states at both the valence band and conduction band, as indicated by the blue arrows, indicating a smaller band gap (1.44 ± 0.03 eV). Moreover, the Fermi level is positioned near the conduction band, indicating the WSe_2/TiOPc stack has n-type characteristics. It is noted that although the TiOPc/WSe_2/HOPG has a smaller band gap than WSe_2/HOPG, there are no midgap states, and deposition of a gate oxide may remove the band edge states since they can be due to weakly bound charge, which is eliminated by oxide bonding.[21] A previous STS of Al_2O_3 deposition on TiOPc/HOPG showed that a few monolayers of Al_2O_3 increased the band gap as measured by STS.

After verifying the TiOPc seeding layer on MBE-grown WSe_2 *via* STM, the Al_2O_3 was deposited on the TiOPc/WSe_2 surface by the ALD process. It is noted that the bulk WSe_2 samples were employed for atomic force microscopy (AFM) and conductive AFM (C-AFM). Uniform deposition of Al_2O_3 on the bulk WSe_2 at 393 K assisted by a TiOPc seeding layer is confirmed by AFM. Figure 2a and b show topographic differences of ALD Al_2O_3 on bulk WSe_2 with and without the TiOPc seeding layer using the same ALD growth conditions. Because the ideal surface of WSe_2 (defect-free surface) does not possess dangling bonds, ALD nucleation occurs at defects or step edges. Figure 2a shows that the resulting surface has 5.5 nm deep pinholes with diameters at the 100 to 500 nm scale and a root-mean-square (RMS) surface roughness of 3.6 nm. In contrast, for the sample that includes a ML TiOPc seeding layer, the Al_2O_3 attaches uniformly on the TiOPc/WSe_2 without pinholes, as shown by the AFM image and the associated line trace in Figure 2b. As a result of the elimination of pinholes in the Al_2O_3/TiOPc/WSe_2 stack, the RMS roughness is decreased by more than a factor of 20 to 0.15 nm. This RMS roughness value is less than one-third of the RMS roughness obtained using a remote O_2 plasma-assisted, 120-cycle ALD Al_2O_3 film on MoS_2.[19]

Integrating the TiOPc seeding layer into the ALD process also decreases the gate leakage current, as shown in Figure 2c. Leakage current was measured by C-AFM in a dark box on a sample for which Al_2O_3 was deposited with and without the TiOPc seed layer, using conductive plateau AFM tips (nanosensors: PL2-NCH). For the sample without TiOPc, the diameter of the AFM tip is sufficiently small (1.8 μm) that it can contact the WSe_2 through pinholes in the Al_2O_3. Because the WSe_2 surface is electrically conductive, the current measured through a pinhole reaches the 10 nA compliance of the system. Conversely, because there are no detectable pinholes in the Al_2O_3/TiOPc/WSe_2 stack, the C-AFM tip contacts only the Al_2O_3 and the leakage current is reduced by more than 2 orders of magnitude. It is noted that the current does not return to zero at 0 V in the Al_2O_3/TiOPc/WSe_2 heterostructure. For a sweep rate from minus to plus 0.5 V/s, the minimum current is observed at 3.5 V, indicating some charging of traps. However, because the traps are likely present on the air-exposed oxide surface, they may be removed during gate metal deposition during FET fabrication. Therefore, the FET measurements described below are the preferred method to quantify the oxide quality.

The uniformly deposited Al_2O_3 and the interface at Al_2O_3 and TiOPc/WSe_2 are observed *via* transmission electron microscopy (TEM). Figure 3 shows the cross-sectional TEM

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX−XXX

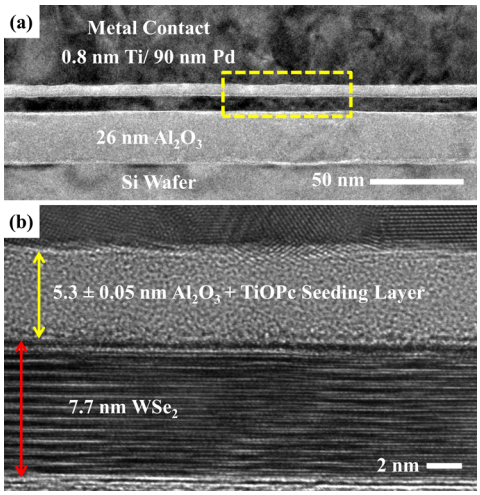


Figure 3. Cross-sectional transmission electron microscopy (TEM) of deposited Al_2O_3/TiOPc stack on exfoliated WSe_2. (a) Low-magnification and (b) high-magnification cross-sectional TEM images of Pd/Ti/Al_2O_3/TiOPc/WSe_2/Al_2O_3/Si. The TEM images were taken from the fabricated device channel cross-section using a focused ion beam. The TEM images indicate that using a seeding layer of TiOPc results in full coverage of the WSe_2 channel with uniform and pinhole-free Al_2O_3 oxide.

images of the Al_2O_3/TiOPc/WSe_2 at two different magnifications. In Figure 3a, the deposited Al_2O_3 oxide fully covers the TiOPc/WSe_2; it is uniform and pinhole free, without observable defects. The thickness of the deposited TiOPc/Al_2O_3 gate dielectric stack is about 5.3 ± 0.05 nm, including the TiOPc seeding layer. It is noted that the given standard error includes the variation of thickness depending on the points in TEM image. Because TiOPc is an organic molecule that scatters electrons weakly, the precise boundary between the amorphous Al_2O_3 dielectric and the TiOPc ML cannot be resolved by TEM. Assuming a TiOPc ML thickness of 0.3 nm[26] between the Al_2O_3 and WSe_2, the deposited Al_2O_3 is 5.0 ± 0.05 nm thick, which is consistent with a 1.0 Å/cycle growth rate. This growth rate is close to the reported 1.1 Å/cycle growth rate of Al_2O_3 deposited *via* ALD on Si(100) at 450 K.[27] It is noted that the growth rate of Al_2O_3 does not depend strongly on temperature: it varies by only 0.1−0.15 Å in the growth temperature range of 373 to 443 K.[27] After deposition of the dielectric on TiOPc/WSe_2, the surface of the WSe_2 remains well-defined, as shown in Figure 3b, indicating that the TiOPc is not reacting with the TMD during deposition.

To extract the dielectric constant of the deposited Al_2O_3, a Ni/Al_2O_3 (50 cycles)/TiOPc/graphene capacitor was fabricated with the same ALD recipe in the Methods section, as outlined in the Supporting Information. Graphene was employed since large-area graphene is available for the fabrication of metal-oxide-graphene capacitors, in contrast to small-domain WSe_2. In Figure S6 in the Supporting Information, the V-shape of the capacitance voltage curves is obtained resulting from the influence of the quantum capacitance of graphene.[28,29] The maximum capacitance density is 1147 nF/cm^2, measured at 1 kHz. It is assumed that the

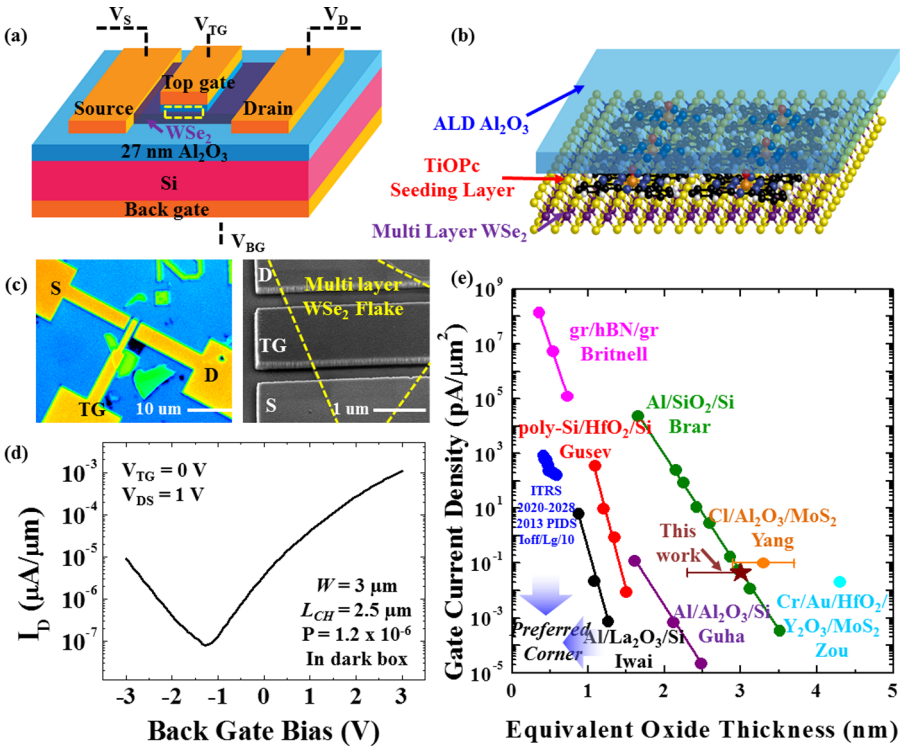


Figure 4. Double-gate WSe_2 FET with Al_2O_3/TiOPc as gate dielectric. (a) Schematic three-dimensional diagram of fabricated device. (b) Schematic diagram of the Al_2O_3/TiOPc/WSe_2 stack from the yellow box of (a). (c) Optical top view micrograph (left) and scanning electron microscope (SEM) image of the FET structure (right) with labels S for source, D for drain, and TG for top gate. The WSe_2 flake is marked by yellow lines. (d) Back-gated transfer characteristic of Al_2O_3/TiOPc/WSe_2/Al_2O_3/Si transistor. The ambipolar characteristic of WSe_2 is observed. (e) Reported gate current density at 1 V for selected high-*k* oxides on Si *vs* best high-*k* oxides on TMDs,[31−38] including this work on Al_2O_3/TiOPc/WSe_2 (brown). The contact metals and channels in the Al_2O_3 oxide gate stacks are different; for completeness, it is noted that Guha[32] used Al/Al_2O_3/Si, Yang[19] used Cr/Al_2O_3/MoS_2, and our stack is Pd/Al_2O_3/TioPc/WSe_2.

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX−XXX

thickness of Al_2O_3 on TiOPc/graphene has identical thickness to Al_2O_3 on TiOPc/WSe_2 (5.3 ± 0.05 nm). Therefore, the static dielectric constant κ = 7.2 ± 0.07 and the equivalent oxide thickness is 3.0 nm, using $C_{OX} = \varepsilon_O\kappa/t_{OX}$. It is noted that TiOPc has about a 1.1−1.3 dielectric constant with about a 0.3 nm thickness; therefore the impact of the TiOPc seeding layer on the capacitance C_{max} is nearly negligible.[30]

FET Gate Stacks on Exfoliated WSe_2. FETs were fabricated by depositing 50 ALD cycles of Al_2O_3 on exfoliated multilayer WSe_2, with a seeding monolayer of TiOPc, as discussed earlier and illustrated in the schematic diagrams of Figure 4a and b. It is noted that although the exfoliated multilayer WSe_2 has a smaller band gap than the MBE-grown ML of WSe_2, the desorption temperatures of TiOPc for both the exfoliated multilayer of WSe_2 and the MBE-grown ML WSe_2 are nearly identical because the TiOPc seeding layer relies on nonbonding van der Waal interactions with WSe_2. Therefore, since the TiOPc interaction strengths with the WSe_2 ML and multilayer are nearly identical, it can be hypothesized that both the TiOPc seed layers on these two surfaces would have similar ALD reaction behavior.

Optical and scanning electron micrographs of one FET are shown in Figure 4c. The transistors are center-gated, and the electrical results were taken on four transistors with device geometries summarized in Table 1. Transfer characteristics (I_D *vs* V_{BG}), shown in Figure 4d, were measured under vacuum and in the dark at 300 K. The ambipolar behavior results from electron accumulation at positive bias and hole accumulation at negative back-gate bias. As the back-gate bias increases from −3 to −1.3 V, the drain current decreases by 2 orders of magnitude due to reduction of hole injection into the WSe_2 channel. As back-gate bias continues to increase from −1.3 to 3 V, the drain current increases by 4 orders of magnitude, resulting from injection of electrons. The minimum current occurs at a negative voltage, suggesting a positive interfacial charge in the underlying Al_2O_3, giving rise to n-type conductivity at zero back-gate bias. The highest current density is obtained in the electron branch, 1 nA/μm. This low current density suggests that the on-current is limited by the Schottky contact and not the transistor. It is noted that the on/off ratio of 10^4 obtained here on an 11 ML WSe_2 channel can be expected to increase to 10^6 by reducing the channel thickness to 1 ML as obtained by Liu.[13] The on-current observed here using the Pd/Ti/WSe_2 contact is approximately 1 nA/μm at V_{DS} = 1 V and V_{BG} = 3 V. This is comparable to the finding of Liu for Ti/WSe_2 of 7 nA/μm at V_{DS} = 1 V and V_{BG} = 30 V. The ambipolar characteristic of multilayer WSe_2 agrees with prior reports.[8,11]

The 5.3 ± 0.05 physical layer thickness of the Al_2O_3/TiOPc/WSe_2 FET reported here has a leakage current density of 0.046 pA/μm^2 at 1 V gate bias. There is uncertainty in the value of the relative dielectric constant for Al_2O_3. The error bar shown in Figure 4e places the dielectric constant in the range 7−9. The value of 7 is obtained from a separate single measurement of ALD Al_2O_3 grown under nominally the same conditions on graphene. This dielectric constant value corresponds to an EOT of 3 nm. The range 7−9 for the dielectric constant corresponds to the range 2.3−3 nm for EOT. The relative dielectric constant of ε_r = 9 was used in our early report where an EOT of 2.2 nm was reported on a film with an estimated physical thickness of 5 nm.[31]

Figure 4e benchmarks the measured gate current density from prior oxide reports[32−38] on Si and best high-*k* oxides on TMDs, including the present result on WSe_2. All the results were obtained at 1 V, except Yang's report on MoS_2, which was obtained at 3 V. It is noted that different metal contacts have different alignment of their Fermi levels with respect to the conduction and valence bands, resulting in different barrier heights for electron/hole transport. Therefore, the metal contacts employed in each case are specified in Figure 4e.

There are few gate current reports on thin TMD gate stacks. Britnell[37] reported the gate current density in graphene/hexagonal boron nitride (h-BN)/graphene stacks for 1 to 4 MLs of h-BN. While the EOT of BN is the lowest of any TMD gate dielectric, the gate current density of Britnell's report far exceeds device targets set by the International Technology Roadmap for Semiconductors (ITRS).[39] The best prior report of a high-*k* oxide/TMD gate stack is the Al_2O_3 on MoS_2 by Yang, with an EOT in the range 2.9 to 3.7 nm, assuming that the dielectric constant is in the range 7 to 9.[19] The reported gate current density in Yang's oxide was 0.1 pA/μm^2 measured at 3 V. While Zou's current density for HfO_2/Y_2O_3 on MoS_2 is 2 times smaller than the current density reported in this work, the EOT is more than 1.4 times larger. Because the leakage current increases exponentially as the dielectric thickness decreases, the result shows that the TiOPc seeding process on WSe_2 successfully scales the EOT without sacrificing the leakage current density. The present measurements using the TiOPc functionalization layer stand as the lowest measured gate current density with EOT below 3 nm achieved to date on TMDs.

The top-gate FET transfer characteristics are displayed in Figure 5 for a device with a channel length of L_{CH} = 2.4 μm, width of W = 4.5 μm, and gate-to-drain and gate-to-source spacing of $L_{GD} = L_{GS}$ = 450 nm. The back gate is biased to obtain (a) n-channel or (c) p-channel FET transfer characteristics. The corresponding band diagrams shown in Figure 5b and d provide a self-consistent explanation of the observed characteristics. Referring to band diagrams in Figure 5b and d, maximum currents are limited by the reverse-biased Schottky barriers, and the minimum currents are obtained when the gate bias raises the channel barrier potential above the controlling Schottky barrier. A subthreshold swing of 133 mV/decade is obtained in the electron branch with an on/off current ratio as high as 5 × 10^4. The p-FET characteristic has on/off ratio of 100 with a higher subthreshold swing of 390 mV/decade.

A lower subthreshold swing of 80 mV/decade was obtained on a device with L_{CH} = 2.2 μm, W = 3 μm, and $L_{SG} = L_{DG}$ = 350 nm, as shown in Figure 6a. Since the gate oxide was the same on these devices, the improvement is likely related to lower interface trap density or variability in thicknesses from flake to flake. Double sweep measurements with a sweep rate of 54 mV/s show that forward and backward sweeps, expanded in Figure 6b, differ by a maximum value of 40 mV. From this shift and using the geometrical capacitance of the gate stack a trap density of approximately 2.8 × 10^{11} /cm^2 is achieved. It is noted that subthreshold swings as low as 60 mV/decade have been reported by Fang[12] on a monolayer WSe_2 p-FET with NO_2

Table 1. Summary of Exfoliated WSe_2 FETs Geometries

FET	L_{CH} (μm)	W (μm)	$L_{GD} = L_{GS}$ (μm)	measurements
1	2.5	3	0.5	$I_D - V_{BG}$
2	2.4	4.5	0.45	I_D, $I_{TG} - V_{TG}$
3	2.2	3	0.35	subthreshold swing
4	0.58	3	0.4	$I_D - V_{TG}$ breakdown

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX−XXX

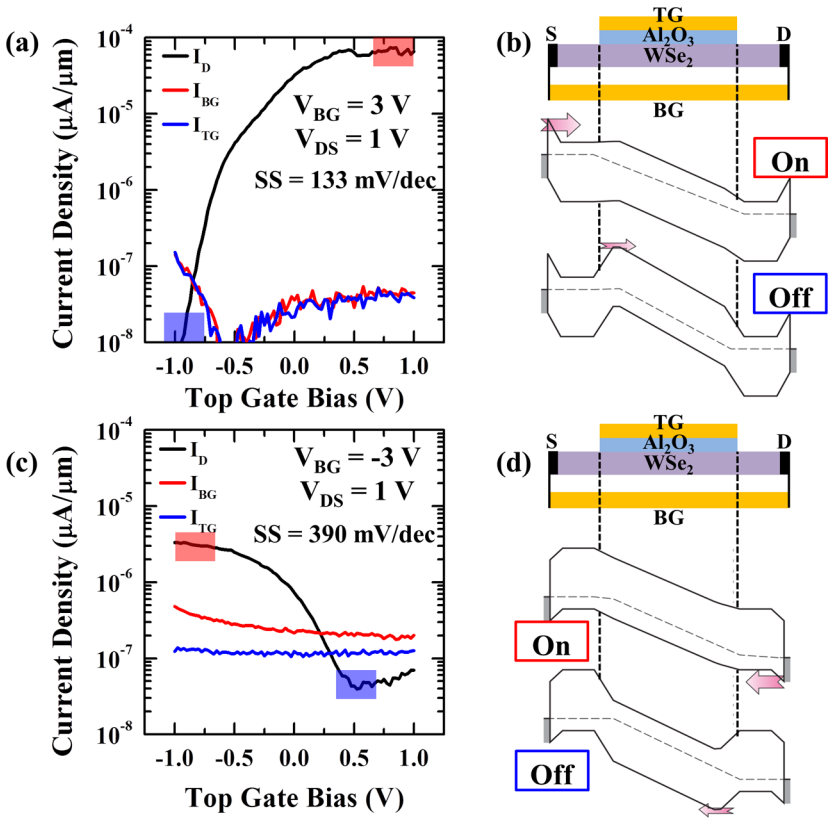


Figure 5. Electrical characteristics of a top-gated WSe_2 FET with TiOPc/Al_2O_3 gate stack. (a) Transfer characteristics and top-gate leakage current *vs* top-gate bias of an n-FET that has a top gate to source/drain spacing of 450 nm, a gate length L_{CH} = 2.4 μm, and W = 4.5 μm, when biased as an n-FET. Measurements were made in a vacuum probe station in the dark. (b) Energy diagram of a corresponding n-FET mode. (c) Transfer characteristics and top-gate leakage current *vs* top-gate bias of a p-FET in the same device. (d) Energy diagram of a corresponding p-FET mode.

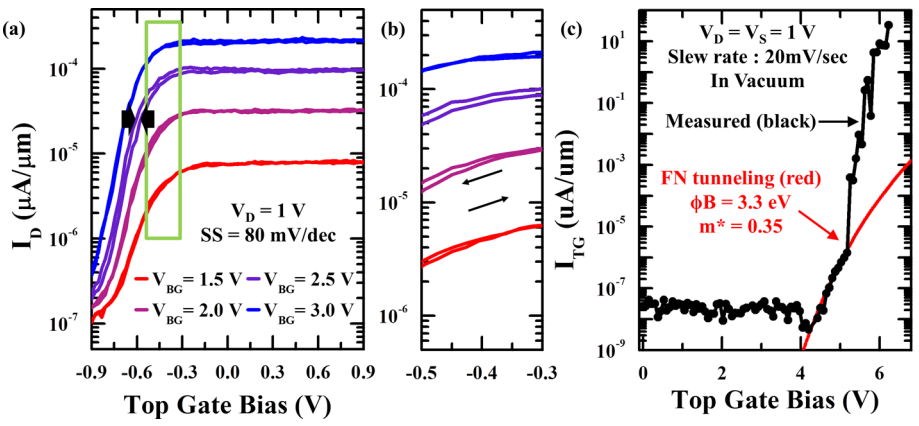


Figure 6. (a) Top-gated WSe_2 FET with TiOPc/Al_2O_3 gate stack biased as the n-FET mode, (b) expanded view showing hysteresis with a sweep rate of 54 mV/s, and (c) current density *vs* top-gate voltage through breakdown. The 80 mV/decade subthreshold swing in (a) was obtained on a device with L_{CH} = 2.2 um, W = 3 μm, and L_{SG} = L_{DG} = 350 nm. The breakdown voltage characterization was made on a FET with L_{CH} = 580 nm, W = 3 μm, and L_{SG} = L_{DG} = 40 nm, with V_D = V_S = 0 V.

doping of the contact regions. Therefore, it can be hypothesized that the subthreshold swing of Al_2O_3/TiOPc/WSe_2 can be further decreased by employing a single layer of WSe_2 and a proper doping process on S/D regions.

To obtain the breakdown voltage, drain and source voltages were set to zero, while the top-gate voltage was swept between 0 and 6 V. This measurement was done on a device with L_{CH} = 580 nm, W = 3 μm, and L_{SG} = L_{DG} = 40 nm. Figure 6c shows an I–V characteristic at the noise floor of the instrument until a voltage of approximately 4 V is reached. At 4 V the characteristics follow a Fowler–Nordheim behavior,[40] which can be fitted to obtain effective mass and barrier height as shown in Figure 6c. The values of 3.3 eV for barrier height and 0.35 for effective mass are consistent with prior estimates.[41−44] At approximately 5 V the breakdown field of the oxide is reached, corresponding to approximately 10 MV/cm. This is higher than the best prior report on breakdown field of a high-k

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX−XXX

oxide on epitaxial graphene (8 nm HfO_2/2 nm Al_2O_3)[45] and MoS_2 (HfO_2/Y_2O_3),[38] 7 and 4.5 MV/cm, respectively.

CONCLUSION

A scalable ALD gate process for WSe_2 is shown, which uses TiOPc as a seeding layer. STM measurements show that TiOPc molecules tile uniformly without pinholes on WSe_2 with 4-fold symmetry. Because TiOPc molecules can provide multiple high binding energy adsorption sites to TMA, uniform deposition of Al_2O_3 is obtained without noticeable pinholes, as shown by AFM. Due to the elimination of pinholes in the deposited Al_2O_3 on TiOPc/WSe_2, the leakage current measured by gateless conductive AFM is reduced by over 2 orders of magnitude compared to Al_2O_3/WSe_2. To evaluate the quality of the deposited dielectric, FETs were fabricated on multilayer WSe_2. The top-gated WSe_2 FET possesses an EOT of 3.0 nm and leakage current of 0.046 pA/μm^2 at 1 V gate bias. This leakage current is lower than previous deposited dielectrics on TMD materials with reasonably low EOT. The barrier height of 3.3 eV is extracted from Fowler–Nordheim $I-V$ characteristics near breakdown for the Al_2O_3/TiOPc/WSe_2 gate stack. The process is broadly extensible to graphene, WSe_2 and related materials, and other transistors, such as tunnel FETs.

METHODS

The initial process development in the seeding layer deposition for this paper utilized WSe_2 grown by MBE on HOPG. Although the fabrication of the device can be performed on exfoliated WSe_2, since it is extremely difficult to perform STM/STS with a few micrometer sized exfoliated WSe_2 flakes, MBE-grown WSe_2/HOPG has been employed for STM and STS. The WSe_2 layers were deposited by MBE in an ultra-high-vacuum system (RIBER, MBE 32) on the HOPG; the HOPG samples were cleaned by multiple exfoliation, before transferring the HOPG sample into the UHV chamber, Afterward, the HOPG samples were gradually heated to 1073 K with a 70 K/min heating rate; then the growth temperature was held at 1073 K for 20 min. Once the growth temperature equilibrated at 1073 K, elemental W from an electron beam source and elemental Se from a Knudsen cell were dosed onto the HOPG substrates simultaneously. After deposition of WSe_2 on the HOPG samples, WSe_2/HOPG samples were cooled from 1073 to 670 K to deposit a Se capping layer on the WSe_2/HOPG. Thick Se capping layers (20 nm) were employed to prevent oxidation of the MBE WSe_2/HOPG during wafer transfer to a low-vacuum container (20 mTorr) from the MBE chamber to the STM/STS chamber (from U. Notre Dame to UC San Diego). After transferring the WSe_2/HOPG into the UHV (Omicron, base pressure $<1 \times 10^{-10}$ Torr), samples were annealed at 750 K for 120 min to remove the Se cap and ambient adsorbates.

The MBE deposition of single TiOPc MLs was performed with a differentially pumped effusion cell (Eberl MBE - Komponenten), attached to the Omicron UHV chamber. During deposition of the TiOPc seeding layer, WSe_2 samples were held at 373 K in the UHV chamber (1×10^{-10} Torr), while the TiOPc source was sublimated at 633 K in the effusion cell (2×10^{-6} Torr). Subsequently, the multilayers were annealed at 473 K for 6 min to obtain a flat-lying ML of TiOPc as determined by STM. All STM and STS were performed at 100 K in a variable-temperature STM system (base pressure 5×10^{-11} Torr) using electrochemically etched tungsten tips.

For top-gated FETs, exfoliated WSe_2 was employed (2D Semiconductors). Back contacts were deposited by electron-beam evaporation of Ti/Au (5 nm/100 nm) onto the p^+ Si wafer. On the top surface, 27 nm of Al_2O_3 was deposited by ALD. Multilayer WSe_2 flakes were exfoliated onto the 27 nm Al_2O_3 layer. The source/drain contacts were patterned on the flakes for source/drain contacts using electron-beam lithography (EBL) followed by electron-beam deposition of Ti/Pd (0.8/90 nm) and lift off. To functionalize the surface for ALD, a ML of TiOPc was deposited on WSe_2 by organic MBE, using the system referred to above. As described above, after deposition of thick TiOPc layers on WSe_2 FETs, TiOPc/WSe_2/Al_2O_3/Si FETs were annealed at 473 K for 6 min to obtain a single TiOPc ML on the WSe_2/Al_2O_3/Si FETs. Afterward, the TiOPc/WSe_2 FETs were transferred to the ALD reactor in air within 10 min.

Deposition of Al_2O_3 was performed in a commercial ALD chamber (Beneq model TFS 200). In the Beneq tool, ALD was initiated by dosing of 50 TMA prepulses, followed by ALD of Al_2O_3, while the WSe_2 samples were held at 393 K. The TiOPc seeding layer can be desorbed from WSe2 at 473 K; therefore, this sets a limit on the ALD temperature. The pulse sequence and times used were 200 ms TMA, 6 s N_2 purge, 50 ms H_2O, and 6 s N_2 purge, repeated 50 cycles. No postdeposition anneal of the FET gate stack was performed. Finally, the top gate contacts were patterned using EBL, followed by thermal evaporation of 160 nm of Pd and lift off. The device measurements of fabricated FETs were carried out in a vacuum probe station at a pressure of 1.2×10^{-6} Torr in the dark box.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b02648.

Experimental details (ALD, STS, and fabrication of capacitors and devices), ALD deposition on other 2D materials, XPS, and KPFM (PDF)

AUTHOR INFORMATION

Corresponding Authors

*E-mail: Sara.Fathipour.1@nd.edu.
*E-mail: seabaugh.1@nd.edu.
*E-mail: akummel@ucsd.edu.

Author Contributions

¶J. H. Park and S. Fathipour contributed equally to this publication.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work is supported in part by the National Science Foundation Grant DMR 1207213, by the Center for Low Energy Systems Technology (LEAST), a STARnet Semiconductor Research Corporation (SRC) program sponsored by MARCO and DARPA, and by the SRC Nanoelectronic Research initiated through the South West Academy of Nanoelectronics (SWAN).

REFERENCES

(1) Sze, S. M. *Physics of Semiconductor Devices*; Wiley-Interscience: New York, 1969.

(2) Sakurai, T. Perspectives of Low-Power VLSI's. *IEICE T Electron* **2004**, *E87c*, 429–436.

(3) Suzuki, E.; Ishii, K.; Kanemaru, S.; Maeda, T.; Tsutsumi, T.; Sekigawa, T.; Nagai, K.; Hiroshima, H. Highly Suppressed Short-Channel Effects in Ultrathin SOI n-MOSFET's. *IEEE Trans. Electron Devices* **2000**, *47*, 354–359.

(4) Yee Chia, Y.; Subramanian, V.; Kedzierski, J.; Peiqi, X.; Tsu-Jae, K.; Bokor, J.; Chenming, H. Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel. *IEEE Electron Device Lett.* **2000**, *21*, 161–163.

(5) Luisier, M.; Lundstrom, M.; Antoniadis, D. A.; Bokor, J. Ultimate Device Scaling: Intrinsic Performance Comparisons of Carbon-Based, InGaAs, and Si Field-Effect Transistors for 5 nm Gate Length. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, Dec 5–7, 2011; IEEE, 2011; pp 11.2.1–11.2.4.10.1109/IEDM.2011.6131531

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX–XXX

(6) Ernst, T.; Cristoloveanu, S.; Ghibaudo, G.; Ouisse, T.; Horiguchi, S.; Ono, Y.; Takahashi, Y.; Murase, K. Ultimately Thin Double-Gate SOI MOSFETs. *IEEE Trans. Electron Devices* **2003**, *50*, 830−838.
(7) Jena, D. Tunneling Transistors Based on Graphene and 2-D Crystals. *Proc. IEEE* **2013**, *101*, 1585−1602.
(8) Das, S.; Appenzeller, J. WSe_2 Field Effect Transistors with Enhanced Ambipolar Characteristics. *Appl. Phys. Lett.* **2013**, *103*, 103501.
(9) Jones, A. M.; Yu, H. Y.; Ghimire, N. J.; Wu, S. F.; Aivazian, G.; Ross, J. S.; Zhao, B.; Yan, J. Q.; Mandrus, D. G.; Xiao, D.; Yao, W.; Xu, X. D. Optical Generation of Excitonic Valley Coherence in Monolayer WSe_2. *Nat. Nanotechnol.* **2013**, *8*, 634−638.
(10) Wu, S. F.; Buckley, S.; Schaibley, J. R.; Feng, L. F.; Yan, J. Q.; Mandrus, D. G.; Hatami, F.; Yao, W.; Vuckovic, J.; Majumdar, A.; Xu, X. D. Monolayer Semiconductor Nanocavity Lasers with Ultralow Thresholds. *Nature* **2015**, *520*, 69−U142.
(11) Das, S.; Prakash, A.; Salazar, R.; Appenzeller, J. Toward Low-Power Electronics: Tunneling Phenomena in Transition Metal Dichalcogenides. *ACS Nano* **2014**, *8*, 1681−1689.
(12) Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A. High-Performance Single Layered WSe_2 p-FETs with Chemically Doped Contacts. *Nano Lett.* **2012**, *12*, 3788−3792.
(13) Liu, W.; Kang, J. H.; Sarkar, D.; Khatami, Y.; Jena, D.; Banerjee, K. Role of Metal Contacts in Designing High-Performance Monolayer n-Type WSe_2 Field Effect Transistors. *Nano Lett.* **2013**, *13*, 1983−1990.
(14) Podzorov, V.; Gershenson, M. E.; Kloc, C.; Zeis, R.; Bucher, E. High-Mobility Field-Effect Transistors Based on Transition Metal Dichalcogenides. *Appl. Phys. Lett.* **2004**, *84*, 3301−3303.
(15) Chen, K.; Kiriya, D.; Hettick, M.; Tosun, M.; Ha, T. J.; Madhvapathy, S. R.; Desai, S.; Sachid, A.; Javey, A. Air Stable n-Doping of WSe_2 by Silicon Nitride Thin Films with Tunable Fixed Charge Density. *APL Mater.* **2014**, *2*, 092504.
(16) Liu, H.; Xu, K.; Zhang, X. J.; Ye, P. D. The Integration of High-k Dielectric on Two-Dimensional Crystals by Atomic Layer Deposition. *Appl. Phys. Lett.* **2012**, *100*, 152115.
(17) Azcatl, A.; McDonnell, S.; Santosh, K. C.; Peng, X.; Dong, H.; Qin, X. Y.; Addou, R.; Mordi, G. I.; Lu, N.; Kim, J.; Kim, M. J.; Cho, K.; Wallace, R. M. MoS_2 Functionalization for Ultra-Thin Atomic Layer Deposited Dielectrics. *Appl. Phys. Lett.* **2014**, *104*, 111601.
(18) Cheng, L. X.; Qin, X. Y.; Lucero, A. T.; Azcatl, A.; Huang, J.; Wallace, R. M.; Cho, K.; Kim, J. Atomic Layer Deposition of a High-k Dielectric on MoS_2 Using Trimethylaluminum and Ozone. *ACS Appl. Mater. Interfaces* **2014**, *6*, 11834−11838.
(19) Yang, W.; Sun, Q. Q.; Geng, Y.; Chen, L.; Zhou, P.; Ding, S. J.; Zhang, D. W. The Integration of Sub-10 nm Gate Oxide on MoS_2 with Ultra Low Leakage and Enhanced Mobility. *Sci. Rep.* **2015**, *5*, 11921.
(20) Azcatl, A.; Santosh, K. C.; Peng, X.; Lu, N.; McDonnell, S.; Qin, X. Y.; de Dios, F.; Addou, R.; Kim, J.; Kim, M. J.; Cho, K.; Wallace, R. M. HfO_2 on UV-O_3 Exposed Transition Metal Dichalcogenides: Interfacial Reactions Study. *2D Mater.* **2015**, *2*, 014004.
(21) Park, J. H.; Movva, H. C. P.; Chagarov, E.; Sardashti, K.; Chou, H.; Kwak, I.; Hu, K. T.; Fullerton-Shirey, S. K.; Choudhury, P.; Banerjee, S. K.; Kummel, A. C. *In Situ* Observation of Initial Stage in Dielectric Growth and Deposition of Ultrahigh Nucleation Density Dielectric on Two-Dimensional Surfaces. *Nano Lett.* **2015**, *15*, 6626−6633.
(22) Podberezskaya, N. V.; Magarill, S. A.; Pervukhina, N. V.; Borisov, S. V. Crystal Chemistry of Dichalcogenides MX_2. *J. Struct. Chem.* **2001**, *42*, 654−681.
(23) Kera, S.; Yabuuchi, Y.; Yamane, H.; Setoyama, H.; Okudaira, K. K.; Kahn, A.; Ueno, N. Impact of an Interface Dipole Layer on Molecular Level Alignment at an Organic-Conductor Interface Studied by Ultraviolet Photoemission Spectroscopy. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2004**, *70*, 085304.
(24) Norton, J. E.; Bredas, J. L. Theoretical Characterization of Titanyl Phthalocyanine as a p-Type Organic Semiconductor: Short Intermolecular pi-pi Interactions Yield Large Electronic Couplings and Hole Transport Bandwidths. *J. Chem. Phys.* **2008**, *128*, 034701.
(25) Fukagawa, H.; Yamane, H.; Kera, S.; Okudaira, K. K.; Ueno, N. Experimental Estimation of the Electric Dipole Moment and Polarizability of Titanyl Phthalocyanine using Ultraviolet Photoelectron Spectroscopy. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2006**, *73*, 041302.
(26) Lu, X.; Hipps, K. W.; Wang, X. D.; Mazur, U. Scanning Tunneling Microscopy of Metal Phthalocyanines: d(7) and d(9) Cases. *J. Am. Chem. Soc.* **1996**, *118*, 7197−7202.
(27) Groner, M. D.; Fabreguette, F. H.; Elam, J. W.; George, S. M. Low-Temperature Al_2O_3 Atomic Layer Deposition. *Chem. Mater.* **2004**, *16*, 639−645.
(28) Xia, J. L.; Chen, F.; Li, J. H.; Tao, N. J. Measurement of the Quantum Capacitance of Graphene. *Nat. Nanotechnol.* **2009**, *4*, 505−509.
(29) Xia, J. L.; Chen, F.; Tedesco, J. L.; Gaskill, D. K.; Myers-Ward, R. L.; Eddy, C. R.; Ferry, D. K.; Tao, N. J. The Transport and Quantum Capacitance Properties of Epitaxial Graphene. *Appl. Phys. Lett.* **2010**, *96*, 505−509.
(30) Fukagawa, H.; Hosoumi, S.; Yamane, H.; Kera, S.; Ueno, N. Dielectric Properties of Polar-Phthalocyanine Monolayer Systems with Repulsive Dipole Interaction. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2011**, *83*, 085304.
(31) Fathipour, S.; Jun Hong, P.; Kummel, A.; Seabaugh, A. Low-leakage WSe_2 FET gate-Stack Using Titanyl Phthalocyanine Seeding Layer for Atomic Layer Deposition of Al_2O_3. In *Device Research Conference (DRC), 2015 73rd Annual*, June 21−24, 2015; DRC, 2015; pp 213−214.
(32) Brar, B.; Wilk, G. D.; Seabaugh, A. C. Direct Extraction of the Electron Tunneling Effective Mass in Ultrathin SiO_2. *Appl. Phys. Lett.* **1996**, *69*, 2728−2730.
(33) Guha, S.; Cartier, E.; Bojarczuk, N. A.; Bruley, J.; Gignac, L.; Karasinski, J. High-Quality Aluminum Oxide Gate Dielectrics by Ultra-High-Vacuum Reactive Atomic-Beam Deposition. *J. Appl. Phys.* **2001**, *90*, 512−514.
(34) Gusev, E. P.; Buchanan, D. A.; Cartier, E.; Kumar, A.; DiMaria, D.; Guha, S.; Callegari, A.; Zafar, S.; Jamison, P. C.; Neumayer, D. A.; Copel, M.; Gribelyuk, M. A.; Okorn-Schmidt, H.; D'Emic, C.; Kozlowski, P.; Chan, K.; Bojarczuk, N.; Ragnarsson, L. A.; Ronsheim, P.; Rim, K.; Fleming, R. J.; Mocuta, A.; Ajmera, A. Ultrathin High-K Gate Stacks for Advanced CMOS Devices. In *Electron Devices Meeting, 2001, IEDM '01. Technical Digest*; International, Dec 2−5, 2001; IEDM, 2001; pp 20.1.1−20.1.4.
(35) Iwai, H.; Ohmi, S.; Akama, S.; Ohshima, C.; Kikuchi, A.; Kashiwagi, I.; Taguchi, J.; Yamamoto, H.; Tonotani, J.; Kim, Y.; Ueda, I.; Kuriyama, A.; Yoshihara, Y. Advanced Gate Dielectric Materials for sub-100 nm CMOS. In *Electron Devices Meeting, 2002. IEDM '02*; International, Dec 8−11, 2002; IEDM, 2002; pp 625−628.
(36) Burek, G. J.; Hwang, Y.; Carter, A. D.; Chobpattana, V.; Law, J. J. M.; Mitchell, W. J.; Thibeault, B.; Stemmer, S.; Rodwell, M. J. W. Influence of Gate Metallization Processes on the Electrical Characteristics of High-k/In(0.53)Ga(0.47)As Interfaces. *J. Vac Sci. Technol. B* **2011**, *29*, 040603.
(37) Britnell, L.; Gorbachev, R. V.; Jalil, R.; Belle, B. D.; Schedin, F.; Katsnelson, M. I.; Eaves, L.; Morozov, S. V.; Mayorov, A. S.; Peres, N. M. R.; Neto, A. H. C.; Leist, J.; Geim, A. K.; Ponomarenko, L. A.; Novoselov, K. S. Electron Tunneling through Ultrathin Boron Nitride Crystalline Barriers. *Nano Lett.* **2012**, *12*, 1707−1710.
(38) Zou, X.; Wang, J.; Chiu, C.-H.; Wu, Y.; Xiao, X.; Jiang, C.; Wu, W.-W.; Mai, L.; Chen, T.; Li, J.; Ho, J. C.; Liao, L. Interface Engineering for High-Performance Top-Gated MoS_2 Field-Effect Transistors. *Adv. Mater.* **2014**, *26*, 6255−6261.
(39) ITRS. *ITRS*, 2013 ed.; PIDS 2013 tables; 2013.
(40) Fowler, R. H.; Nordheim, L. Electron Emission in Intense Electric Fields. *Proc. R. Soc. London, Ser. A* **1928**, *119*, 173−181.
(41) Yeo, Y. C.; King, T. J.; Hu, C. M. Metal-Dielectric Band Alignment and Its Implications for Metal Gate Complementary Metal-Oxide-Semiconductor Technology. *J. Appl. Phys.* **2002**, *92*, 7266−7271.

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX−XXX

(42) Huang, M. L.; Chang, Y. C.; Chang, C. H.; Lin, T. D.; Kwo, J.; Wu, T. B.; Hong, M. Energy-Band Parameters of Atomic-Layer-Deposition Al_2O_3/InGaAs Heterostructure. *Appl. Phys. Lett.* **2006**, *89*, 012903.
(43) Cowell, E. W.; Muir, S. W.; Keszler, D. A.; Wager, J. F. Barrier Height Estimation of Asymmetric Metal-Insulator-Metal Tunneling Diodes. *J. Appl. Phys.* **2013**, *114*, 213703.
(44) McDonnell, S.; Azcatl, A.; Addou, R.; Gong, C.; Battaglia, C.; Chuang, S.; Cho, K.; Javey, A.; Wallace, R. M. Hole Contacts on Transition Metal Dichalcogenides: Interface Chemistry and Band Alignments. *ACS Nano* **2014**, *8*, 6265−6272.
(45) Sangwan, V. K.; Jariwala, D.; Filippone, S. A.; Karmel, H. J.; Johns, J. E.; Alaboson, J. M. P.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C. Quantitatively Enhanced Reliability and Uniformity of High-kappa Dielectrics on Graphene Enabled by Self-Assembled Seeding Layers. *Nano Lett.* **2013**, *13*, 1162−1167.

DOI: 10.1021/acsnano.6b02648
ACS Nano XXXX, XXX, XXX−XXX