Applied Surface Science 317 (2014) 1022–1027

Contents lists available at ScienceDirect

Applied Surface Science

journal homepage: www.elsevier.com/locate/apsusc

Letter to the Editor

Characterization of interface and border traps in ALD Al_2O_3/GaN MOS capacitors with two-step surface pretreatments on Ga-polar GaN

ARTICLE INFO

Keywords:
Atomic layer deposition (ALD)
Gallium nitride (GaN)
High-k dieletrics
Interface trap density
Border trap density

ABSTRACT

Atomic layer deposited (ALD) Al_2O_3/Ga-polar GaN(0001) metal–oxide–semiconductor (MOS) capacitors have been prepared with surface pretreatments including ex-situ wet sulfide passivation and in-situ cyclic trimethylaluminum (TMA)/hydrogen plasma exposure. Capacitance–voltage characterization showed that the two-step surface preparation led to reductions in the densities of both interface traps and border traps. The influence of the pretreatments on interfacial bonding was investigated by X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS). DFT calculations correlate the electronic properties with the interfacial bonding from the two-step surface preparation. The results are consistent with the surface preparations influencing the nucleation density of the ALD films and, therefore, the defect density of the interface and neighboring oxide.

1. Introduction

GaN-based materials are of particular interest for high power, high frequency and high temperature applications, and GaN-based FETs have demonstrated dramatic increases in output power and efficiency relative to FETs in other semiconductor materials [1]. GaN devices typically employ Schottky gates and are fabricated as High Electron Mobility Transistors (HEMTs). Relatively high gate leakage current in HEMTs has stimulated significant research to develop a GaN metal–oxide (insulator)–semiconductor gate structure in a MOS-HEMT (MIS-HEMT) [2,3]. Metal–insulator–semiconductor transistors (MISFETs) have great potential for enhancement-mode (normally off) operation in power switching systems at MHz frequencies and in analog/digital circuits [4]. Al_2O_3 has been an attractive high-κ dielectric candidate for GaN MOS/MIS devices due to its high breakdown electric field and its favorable band alignment to GaN [5–8]. However, a-Al_2O_3/III–V stacks commonly have higher defect densities than a-SiO_2/Si stacks. Imperfection in the oxide-semiconductor interfacial bonding can lead to a high density of states in the band gaps of either the semiconductor or insulator. These states serve as traps reducing the mobility of the carriers and deteriorate electrostatic control by partially pinning the Fermi-levels in the semiconductor. The interfacial bonding can also influence the formation of defects in the oxide immediately adjacent to the semiconductors; these near-interfacial defects are often denoted as border traps [9,10]. For high-speed MOS/MIS structured GaN devices, an appropriate processing method is needed to have low defect binding between the ALD a-Al_2O_3 and GaN to minimize both the interfacial trap states and the border traps in the near oxide region.

2. Device structure and preparation

Ga-polar GaN layers were grown by metal-organic vapor phase epitaxy (MOVPE) on c-plane sapphire substrates. The MOS structure utilized a 1 μm thick n-GaN layer with Si concentration of $1 \times 10^{17}/cm^3$ grown on a 1.5 μm n+ GaN layer doped with Si at $5 \times 10^{18}/cm^3$, a GaN buffer and sapphire substrate. All GaN samples were first processed at 25 °C with (1) an organic clean consisting of sequential dips in acetone, methanol, and isopropanol and a subsequent 1 min rinse in deionized H_2O and nitrogen blow dry; (2) a 1 min dip in 1:5 (by volume) 37% HCl:H_2O for native oxide removal and a subsequent 1 min rinse in deionized H_2O and nitrogen blow dry; (3) a 1 min dip in 1:2 20% NH_4OH:H_2O and a subsequent 1 min rinse in deionized H_2O and nitrogen blow dry. After step (3), four samples were prepared with further pretreatments before the Al_2O_3 atomic layer deposition, including pretreatment with $(NH_4)_2S$ solution, dosing with TMA, or cyclical exposure to TMA and hydrogen plasma (see Table 1). Details of the ALD in-situ pretreatments and ALD growth conditions have been previously developed and investigated on InGaAs surfaces [11,12] and GaN(0001) [8]. However, the pretreatments' influence on interface and border trap properties of Al_2O_3/GaN MOS has not been studied in detail. For all TMA dosing, the set pressure was 200 mTorr and the Ar carrier gas flow was 100 sccm. For all H_2 plasma dosing, the set pressure was 20 mTorr, the Ar carrier gas flow was 20 sccm, and the H_2 flow was 10 sccm. For all the H_2 stabilization steps, the set pressure was 20 mTorr, the Ar carrier gas flow was 20 sccm and the H_2 flow was10 sccm. For all the H_2O dosing cycles, the set pressure was 200 mTorr and the Ar carrier gas flow was 250 sccm. The samples were held at 300 °C for all in situ pretreatment and ALD steps.

http://dx.doi.org/10.1016/j.apsusc.2014.09.028
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Table 1
Summary of pretreatments (a)–(d) used in this work.

Pretreatment	Soak in sulfide solution	TMA exposure	Cyclic TMA and H_2 plasma exposure
(a)		Yes	
(b)	Yes	Yes	
(c)			Yes
(d)	Yes		Yes

For pretreatment (a), the sample was immediately loaded into the ALD reactor (Oxford Instruments FlexAL ALD), and exposed to five cycles of TMA (in each cycle: TMA pulse = 40 ms, Ar purge = 5 s, and H_2 gas = 10 s). The cycle details are the same as in Ref. [11]. For pretreatment (b), the sample was soaked in 1:3 23%$(NH_4)_2S$:deionized H_2O for 30 min at 50 °C; rinsed with H_2O at 25 °C and blown dry with N_2; immediately afterwards, the sample was loaded into the ALD reactor for the same TMA exposure as in pretreatment (a). For pretreatment (c), the sample was immediately loaded into ALD without the wet sulfide step; the surfaces were in-situ cleaned with five cycles of TMA and hydrogen plasma exposure (in each cycle: 20 mTorr H_2 pulse with inductively coupled plasma power of 100 W for 2 s, followed by 40 ms of TMA, a second hydrogen plasma pulse, followed by 2 s of Ar purge and 10 s of a H_2 stabilization). The cycle details are the same as in Ref. [12]. The remote plasma was turned off during the introduction of TMA pulses so its only function was to produce atomic hydrogen both before and after the TMA doses. For pretreatment (d) the sample received the same wet sulfide step as in pretreatment (b); afterwards, the sample was immediately loaded in the ALD and subjected to the same cyclic TMA and hydrogen plasma clean as in pretreatment (c).

The base pressure of the reactor was approximately 10^{-6} Torr; the pressure was held at 0.2 Torr during the ALD deposition of Al_2O_3. During each cycle of Al_2O_3 growth, TMA was pulsed for 500 ms followed by a 7 s Ar purge, H_2O was pulsed for 500 ms followed by a 7 s Ar purge, the reactor was pumped down for 7 s, followed with an Ar purge at 200 mTorr for 5 s. For *C–V* characterization, samples with 80 such growth cycles were deposited to form Al_2O_3 layers approximately 8 nm thick, while 8 growth cycles were deposited to form ultra-thin oxide layers for XPS and SIMS experiments. *C–V* sample fabrication and characterization was done in two separate runs in order to monitor reproducibility, with results summarized below. The XPS and SIMS results on ultra-thin Al_2O_3/GaN were nearly identical on two sets of samples. For MOS capacitor fabrication, 50-nm-thick palladium gate electrodes were electron-beam evaporated and patterned using a photo-resist lift-off process. To make ohmic contacts, the Al_2O_3 on top of the GaN was removed with 1:10 HF:H_2O for 20 s within a photo-resist patterned area. Then titanium and gold 20/100 nm films were electron-beam evaporated onto the n-doped GaN surface, followed by a lift-off procedure. The samples were not annealed in forming gas.

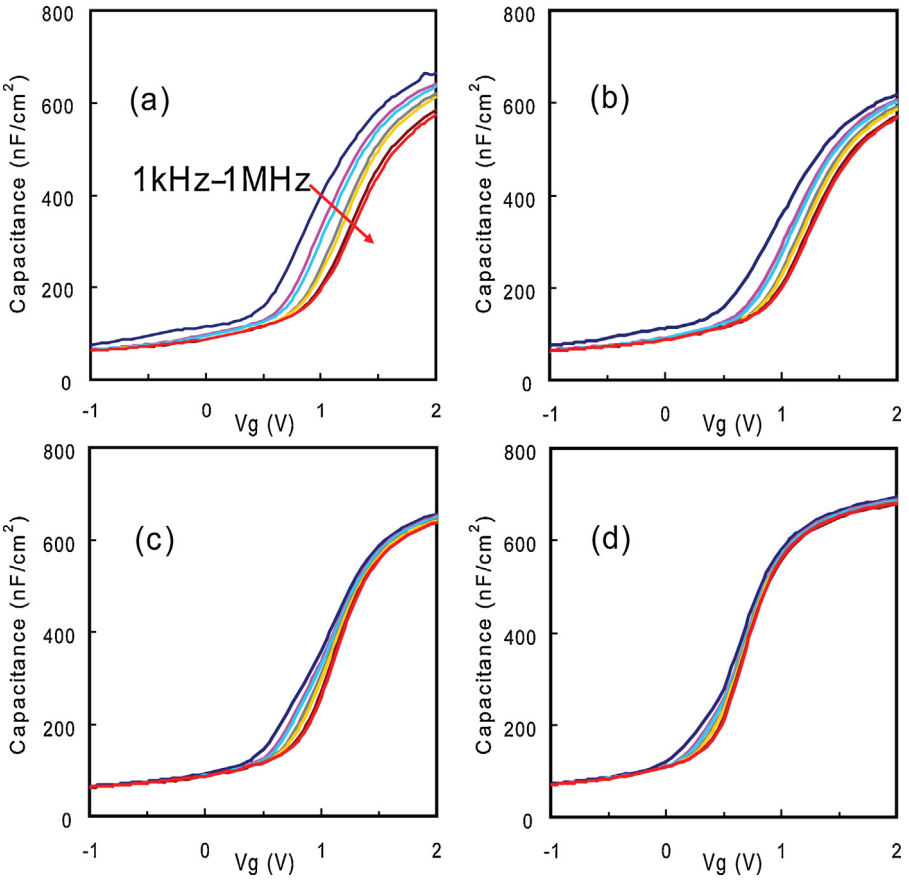

Fig. 1. (a–d) *C–V* characteristics for 80 cycles Al_2O_3/n-GaN MOS capacitors with corresponding surface pretreatments (a)–(d). Curves are shown for measurement frequencies of 1 kHz, 5 kHz, 10 kHz, 50 kHz, 100 kHz, 500 kHz and 1 MHz.

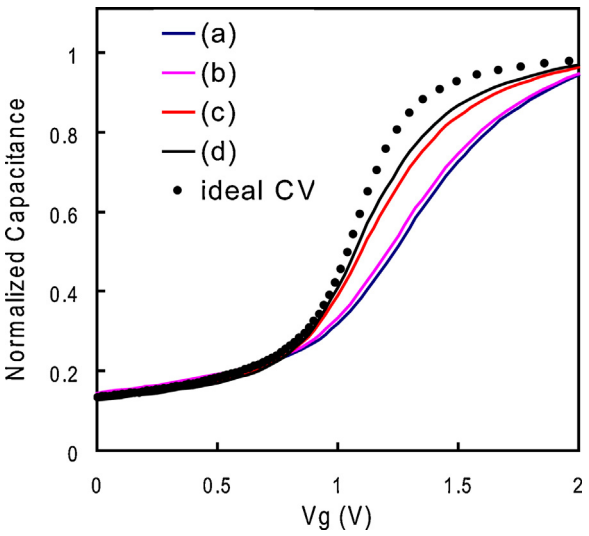

Fig. 2. (a–d) 1 MHz *C–V* curves (solid lines) normalized by extrapolated accumulation capacitances at $V_g = 3$ V for each samples (a)–(d). The *C–V* curve of sample (d) was shifted by 0.4 V toward positive bias to match in the deep depletion. A trap-free 1 MHz *C–V* profile (dots) normalized by its capacitance at 3 V was plotted to illustrate the distortions of experimental *C–V* curves.

3. Measurements and discussion

The *C–V* curves of the MOS capacitors were measured from 1 kHz to1 MHz using an Agilent B1500A Semiconductor Analyzer. For 80 cycles of Al_2O_3 with surface pretreatments (a) to (d), and the corresponding *C–V* curves are shown in Fig. 1. At negative gate biases, the experimental *C–V* curves showed no sign of an inversion layer and little dispersion with frequency due to the small bulk generation-recombination and diffusion-induced inversion from the GaN substrates. The steepness of *C–V* curves as well as the frequency dispersion in the depletion and accumulation regions significantly varied with the surface preparations. In Fig. 2, the 1 MHz *C–V* curves (a)–(d) are compared to an ideal trap-free 1 MHz *C–V* profile (dots). The *C–V* curves were normalized by the extrapolated accumulation capacitance at $V_g = 3$ V in each case. While in-situ pretreament has the greatest effect on *C–V* curves, with the addition of the wet sulfur pretreatment steps ((a) to (b) to (c) to (d)), the measured *C–V* curves demonstrated steeper transitions between depletion and accumulation, as well as reduced deviations from the ideal *C–V*, as expected for a reduction in density of interface traps (D_{it}).

In Fig. 2, the *C–V* curve of sample (d) was shifted by 0.4 V toward positive bias to match the other experimental curves in deep depletion. It was observed that there were flat band voltage shifts between the different sample runs, possibly due to non-reproducibility in the gate metal deposition, which is typically tool specific. Variations of MOS flat-band voltages were calculated by measuring approximately 20 devices on each sample. The standard deviations of the flat-band voltages were typically in the range 80–100 mV. It was confirmed by remeasuring *C–V* curves at 1 kHz after the full set of measurements conducted, that there was little shift ("hysteresis") induced during the measurement process; for example, hysteresis was less than 0.03 V for samples C and D.

The Terman method [13] was employed to estimate D_{it}, since the conductance method is typically not capable of detecting resonant responses of the interface defects for GaN MOS structures [6]. The estimated trap density at 0.5 eV below the conduction band edge varied from (a) 2.8×10^{12}, to (b) 2.0×10^{12}, (c) 1.1×10^{12}, and (d) 0.9×10^{12}/eV/cm^2 in the four samples, with doping set at 1×10^{17}/cm^3. These values are comparable to or lower than previously reported near-band-edge D_{it} estimation on Al_2O_3/GaN

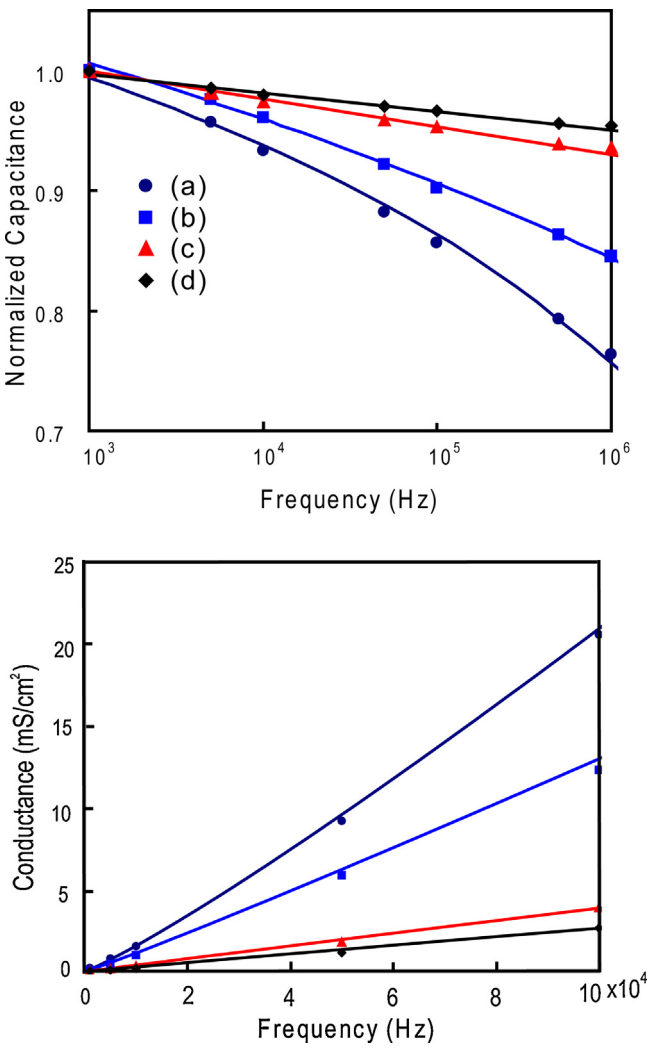

Fig. 3. Top (a–d): Capacitance versus frequency for the four samples in the accumulation region. The capacitance values are normalized at 1 kHz for each sample (colored makers). Bottom (a–d): Conductance versus frequency for the four samples in the accumulation region. The border trap modeling results for both capacitance and conductance (solid lines) are plotted in corresponding colors. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

[7]. To confirm that the differences between samples (c) and (d) were valid, we fit the *C–V* curves on 8 different devices on each sample from the two runs. The relative standard errors in determining these values were calculated to be less than 5%. Mean values of D_{it} and their standard error from the two (c) pretreatment runs were $(10.4 \pm 0.43) \times 10^{11}$ and $(11.5 \pm 0.32) \times 10^{11}$, while those for the (d) pretreatment runs were $(8.81 \pm 0.36) \times 10^{11}$ and $(9.79 \pm 0.31) \times 10^{11}$/eV/cm^2. The difference between the two D_{it} values is confirmed to be significant, with a *p*-value in our two-tailed independent samples *t*-test of 1.1%. In order to extract D_{it} values, oxide capacitance (C_{ox}) estimates were made for each sample by fitting in the accumulation region. The C_{ox} values agreed to within ±9%.

In several earlier theoretical and experimental reports [9,10], strong dispersion in the accumulation region of MOSFET structures with III–V semiconductors were analyzed and assigned to border traps. Using the border trap model described in Ref. [9], the capacitance dispersions for the four sample types were analyzed in the accumulation region when surface potential energies all equaled to 0.12 eV ($V_g = 1.5$ V for sample (a), (b), (c) and $V_g = 1.1$ V for (d)). Fig. 3 shows the capacitances versus frequency for each sample

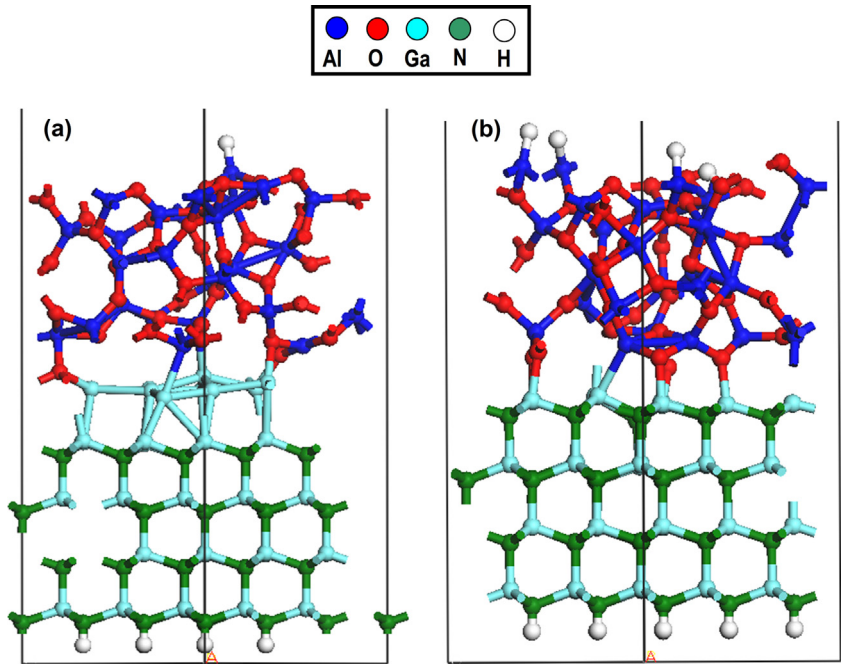

Fig. 4. DFT-MD simulated a-Al_2O_3/GaN(0001) stacks (a) with and (b) without Ga-adlayer between a-Al_2O_3 and GaN.

(colored markers), normalized to the measured capacitance at 1 kHz, and corresponding fitted results using the border trap model (solid lines). The conductance versus frequency (also shown in Fig. 3) was simultaneously fitted to determine both border trap densities and trap time constant. The modeling resulted in estimates of border trap densities of (a) 2.0×10^{20}, (b) 1.0×10^{20}, (c) 3.9×10^{19}, (d) 2.5×10^{19}/eV/cm^3 while the time constant for the traps at the interface (zero-depth traps) slightly varied from 0.8 to 1.3×10^{-7} s. The relative standard errors for the trap densities were calculated to be less than 6% from fitting the *C–V* curves on 8 different devices on each sample. To our knowledge, such quantitative estimates of border traps for GaN MOS devices have not been previously reported [5]. The estimates show that the in-situ cyclic TMA/H_2 procedure in pretreatments (c) and (d) can lead to 80–90% reductions in border trap densities compared to the minimal pretreatment (a). Moreover, wet sulfide pretreatment also had a measurable effect on border trap density, a reduction of border trap densities by a factor of 1.6–2 when comparing pretreatment (b) to (a), or (d) to (c).

To determine the relationship between initiation of oxide growth and trap densities, an XPS study was performed to determine the nucleation density using only 8 cycles of TMA and H_2O to deposit a less than 1 nm Al_2O_3 layer using the same chemical pretreatments as the capacitor structures. Angle-resolved X-ray photoelectron spectroscopy (XPS) of the buried Al_2O_3/GaN interface was performed with an Al Ka source in a Thermo Scientific ThetaProbe. Changes in Ga, Al, N and O XPS signal intensities at the surface were analyzed for the four different surface preparations because the elemental chemical shifts (to be discussed in a separate publication) were small or negligible making peak height analysis more straightforward. The raw data showed that the Al/Ga XPS ratio was much higher for pretreatments (c) and (d), which included the in-situ cyclic TMA/H_2 pretreatment step. Using the Tanuma–Powell–Penn method [14], the oxide thicknesses for 8

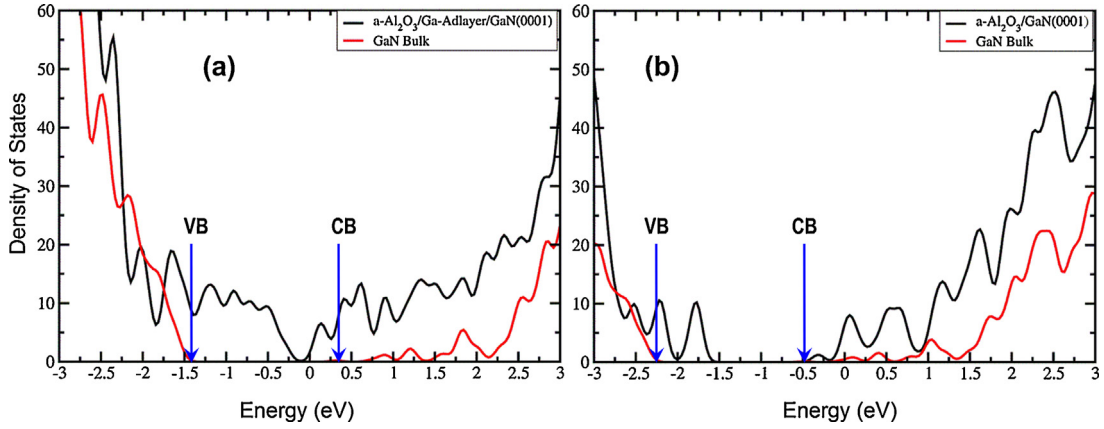

Fig. 5. DFT-simulated DOS curves for a-Al_2O_3/GaN(0001) systems (a) with and (b) without Ga-adlayer between a-Al_2O_3 and GaN(0001). Fermi levels for stack (black) curves are at 0.0 eV for both (a) and (b). DOS curves of GaN bulk unit cell (red curves) were shifted to align deep states with the corresponding stack deep states. Arrows are added to indicate conduction band and valence band for the GaN bulk DOS curves. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

cycle ALD were calculated to be (a) 0.62 nm, (b) 0.56 nm, (c) 0.87 nm, and (d) 0.90 nm. The Cumpson–Seah method [15] derived about 15% lower thickness values but with the same trends. The results are consistent with the TMA/H_2 treatment both cleaning the interface and providing a higher nucleation density for the oxide growth since a high nucleation density results in a significantly thicker oxide coverage in the limit of only a few cycles of ALD oxide deposition. The results are also consistent with interface as well as the border traps being formed in part by poor nucleation of oxide on the GaN surface. One of the factors resulting in improved nucleation associated with the TMA/H_2 treatment may be reduced carbon contamination.

The *C–V* characteristics shown in Fig. 1 are also consistent with a reduction in trap density with sulfide passivation before exposure to air during the transfer to the vacuum ALD chamber. This is consistent with previous reports that after acid/base native oxide removal, ammonium sulfide can avoid native oxide re-formation during air exposure after wet pretreatment [16]. To understand the role of the sulfur layer on the GaN surface during the ALD process, the four samples with 8 ALD cycles were examined with secondary ion mass spectrometry (SIMS) using ION-TOF of V-300 time-of-flight-SIMS tool. A 500 eV Cs^+ beam was employed for sputtering and 15 keV Bi^+ ion beam for analysis (see figure in the supplemental materials). The sulfur ion signals for pretreatments (c) and (d) were noticeably weaker than for (a) and (b). There was no correlation between actual sulfur treatment (pretreatments (b) and (d)) or lack of sulfur treatment (pretreatments (a) and (c)) with sulfur coverage. Instead, the findings are consistent with the H_2 plasma cleaning used in samples (c) and (d) slightly altering the sulfur contamination from atmospheric exposure.

A density functional theory (DFT) study was performed to determine the role of surface chemical treatment of defective sites at high-κ amorphous oxide/Ga-polar GaN interfaces. All DFT simulations were performed with the Vienna Ab-Initio Simulation Package (VASP) [17] using projector augmented-wave (PAW) pseudopotentials (PP) [18] and the PBE (Perdew–Burke–Ernzerhof) exchange-correlation functional [19]. The general procedure of generation and verification of a-Al_2O_3 samples is described in detail elsewhere [20]. While many previously reported DFT simulations of oxide-semiconductor interfaces were limited to artificially formed structures relaxed at 0 K, the present study employed full-scale DFT molecular dynamics (DFT-MD) at finite temperature with amorphous oxide samples, thereby providing the system with enough freedom to naturally evolve into the more realistic states. After initial stacking of the a-Al_2O_3/GaN systems, they were partially relaxed for ~30 conjugate-gradient (CG) relaxation steps, annealed at 800 K for 1000 fs with 1.0 fs timesteps, cooled to 0 K for 200 fs, and finally relaxed below a 0.05 eV/Å force tolerance level. Three bottom layers of GaN slab were permanently fixed in their bulk-like positions. The a-Al_2O_3/GaN(0001) annealed and relaxed samples are shown in Fig. 4(a) and (b). Fig. 4(a) corresponds to a-Al_2O_3/Ga-Adlayer/GaN(0001), while Fig. 4(b) corresponds to the a-Al_2O_3/GaN(0001) stack without Ga-adlayer. Fig. 5 shows the DFT-calculated densities of states (DOS) for a-Al_2O_3/GaN(0001) (black curves) for both (a) and (b) interface configurations, aligned with the DOS of the GaN unit cell (red curves). DOS curves for GaN bulk unit cell (red curves) were shifted in energy to align deep states with the corresponding stack deep states at around −15 eV. Therefore in Fig. 5(a) and (b), energies of 0 eV only refer to the Fermi levels in the oxide/GaN stacks, not in the bulk GaN. The arrows indicate the positions of the conduction band (CB) and valence band (VB) edges in the bulk GaN unit cell. As shown in Fig. 4(a), the inclusion of Ga adlayer significantly shrinks the effective band gap of GaN due to many the Ga–Ga metal–metal bonds, whereas direct stacking of a-Al_2O_3 to GaN without Ga adlayer created a much less pinned interface with wider band gap. There are remaining VB edge states related to the formation of Al-Ga bonds and CB edge states associated with remaining Ga dangling bonds at the oxide/semiconductor interface in this particular sample. Previous studies have shown that the pH of the wet treatments is critical in determining the stability of surface Ga and GaO_x layers [21]. The DFT results show that to achieve a good a-Al_2O_3/GaN(0001) interface, direct bonding between the oxide and the semiconductor is preferable because a-Al_2O_3 can passivate the dangling bonds on the GaN surface primarily through the formation of Ga–O and N–Al bonds. However, a high nucleation density is critical for reducing interfacial trap state density associated with Ga dangling bonds.

4. Conclusion

A two-step pretreatment, which combined wet sulfide passivation with in-situ cyclic trimethylaluminum and hydrogen plasma exposure, was shown to be beneficial in reducing both interface and border traps for Al_2O_3/GaN. Comprehensive DFT-MD simulations of a-Al_2O_3/Ga-polar GaN interfaces were performed to investigate interface formation, bonding structure, and electronic properties at the atomistic level. The experimental (including *C–V*, XPS and SIMS) results along with the simulations were consistent with a high nucleation density reducing the interface dangling bonds responsible for interfacial traps as well as reducing border traps which are thought to be formed in the oxide immediately adjacent to the semiconductor.

Acknowledgements

The authors thank Andrew Carter, Jeremy. J.M. Law, Susanne Stemmer, Brian J. Thibeault, and Mark J.W. Rodwell of University of California, Santa Barbara for helpful discussion and technical supports. A portion of this work was performed in the UCSB nanofabrication facility, which is part of the NSF-funded NNIN network. This work is partially supported by Technology Development Program for Commercializing System Semiconductor by MOTIE, Korea. Addition support was from NSF 1207213 and SRC-LEAST-2383.001 and ONR-N00014-45-4-0078.

Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.apsusc.2014.09.028.

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S. Gu*
Department of Electrical and Computer Engineering, University of California, San Diego, CA 92093, USA

E.A. Chagarov
Department of Chemistry and Biochemistry, University of California, San Diego, CA 92093, USA

J. Min
Department of Electrical and Computer Engineering, University of California, San Diego, CA 92093, USA

S. Madisetti
S. Novak
S. Oktyabrsky
College of Nanoscale Science and Engineering, University at Albany–SUNY, Albany, NY 12148, USA

A.J. Kerr
T. Kaufman-Osborn
A.C. Kummel
Department of Chemistry and Biochemistry, University of California, San Diego, CA 92093, USA

P.M. Asbeck
Department of Electrical and Computer Engineering, University of California, San Diego, CA 92093, USA

* Corresponding author.
E-mail addresses: sigu@eng.ucsd.edu, sigu@ucsd.edu (S. Gu), asbeck@ece.ucsd.edu (P.M. Asbeck).

23 January 2014
Available online 16 September 2014