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Arsenic decapping and pre-atomic layer deposition trimethylaluminum passivation of Al_2O_3/InGaAs(100) interfaces

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The interrelated effects of initial surface preparation and precursor predosing on defect passivation of atomic layer deposited (ALD) Al_2O_3/InGaAs(100) interfaces are investigated. Interface trap distributions are characterized by capacitance-voltage and conductance-voltage analysis of metal-oxide-semiconductor capacitors. Thermal desorption conditions for a protective As_2 layer on the InGaAs surface and dosing conditions of trimethylaluminum prior to ALD-Al_2O_3 are varied to alter the interface trap densities. Experimental results are consistent with the predictions of *ab initio* electronic structure calculations showing that trimethylaluminum dosing of the As-rich $In_{0.53}Ga_{0.47}As(100)$ surface suppresses interface traps by passivating As dangling bonds prior to the initiation of Al_2O_3 deposition. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4818330]

Metal-oxide-semiconductor (MOS) field-effect devices combining III-V semiconductors and deposited high-*k* dielectrics are attracting great interest because of their potential to achieve high carrier mobility and to suppress leakage current in highly scaled devices. However, developing a thermally stable interface with a low density of electrically active defects between a high-*k* gate dielectric and a III-V channel has been a long-standing challenge.[1] $In_{0.53}Ga_{0.47}As$ and atomic layer deposited (ALD) Al_2O_3 are among the leading candidates for high-*k*/III-V n-channel MOS devices because the semiconductor has high electron mobility and a modest band gap that is suitable for future power supply voltage scaling.[2] Furthermore, the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface exhibits a relatively low interface defect density (D_{it}) compared to other deposited high-κ dielectrics on III-V semiconductors.[3,4]

Because III-V arsenide semiconductors have native oxides of poor electrical quality and readily form interface defects,[1] it is desirable to (1) suppress oxidation of the InGaAs surface prior to dielectric deposition and (2) passivate defect sites after dielectric deposition in order to achieve superior transistor performance.[5] Several approaches to prevent oxidation of the III-V semiconductors and to reduce the interface defect density have been reported, including post-deposition forming gas annealing,[6] and pre-deposition sulfur passivation[7] or atomic hydrogen treatment[8] of III-V semiconductor surfaces. It has also been shown that the ALD-Al_2O_3/InGaAs interface defects can be avoided by starting the ALD-Al_2O_3 process with a pulse of trimethylaluminum (TMA), a metal-organic precursor for Al_2O_3 deposition, rather than by initially pulsing an oxidant.[4] As previously reported, TMA can decompose the native oxide on III-V arsenide surfaces[9,10] and protects initially clean III-V surfaces from subsequent oxidation.[4]

In this letter, the effects of large-dose TMA exposure of well-prepared InGaAs(100) surfaces prior to the start of ALD-Al_2O_3 growth are reported. The electrical properties of both n-type and p-type $In_{0.53}Ga_{0.47}As(100)$ prepared under conditions that should result in either As-rich or Ga/In-rich surface structures are compared. The effects of TMA saturation of the substrate surface prior to ALD-Al_2O_3 deposition on the capacitance-voltage and conductance-voltage characteristics of Pd/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors are analyzed. The role of TMA surface adsorption in altering the measured D_{it} distribution across the InGaAs band gap is analyzed using density functional theory (DFT).

Epitaxial $In_{0.53}Ga_{0.47}As(100)$ layers with Si doping ($1 \times 10^{17}\,cm^{-3}$) for n-type or Be doping ($1 \times 10^{17}\,cm^{-3}$) for p-type were covered with an amorphous As_2 capping layer of $80 \sim 100$ nm thickness to protect the InGaAs surface from oxidation during air exposure. The arsenic capping layer was completely removed by thermal desorption (decapping) at approximately 370 °C or 460 °C *in situ* in a high vacuum ALD chamber.[11] The end point of decapping was determined by observation of a completed chamber pressure pulse during As_2 desorption and was previously confirmed by the binding energy shift (−0.7 eV) of As 3*d* peaks measured in x-ray photoelectron spectroscopy. Afterwards, the decapped InGaAs surfaces were dosed with TMA at a substrate temperature of 150 °C or 270 °C prior to ALD-Al_2O_3 deposition. This large-dose TMA exposure consists of 10 cycles of 1 s TMA pulse and 5 s N_2 purge. Approximately 3 nm of Al_2O_3 was deposited using TMA and H_2O (TMA-first in sequence) at a substrate temperature of 270 °C after the TMA treatment. The chamber pressure during the TMA pulse and H_2O pulse was approximately 50 mTorr. The gate metal consisted of 50 nm palladium deposited by thermal evaporation through a shadow mask, and the wafer back side contact consisted of 50 nm Au/20 nm Ti to reduce the contact resistance. Post-metallization forming gas (5% H_2/95% N_2) anneal at atmospheric pressure with a flow rate of 2 l/min was performed for 30 min at 400 °C in a quartz tube furnace. The primary effect of this anneal is to suppress frequency dispersion of the capacitance associated with border traps in the Al_2O_3;[6] however, it also passivates traps associated with defects present at the Al_2O_3/InGaAs interface after formation

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of the MOS capacitors.[12] Multi-frequency capacitance-voltage (C-V) curves were measured in the frequency range from 1 kHz to 1 MHz at room temperature in the dark, using a HP4284A LCR meter.

Figure 1 plots multi-frequency C-V curves for the MOS capacitors fabricated on n-type and p-type InGaAs(100) surfaces which were decapped at 370 °C (low-T decap) and 460 °C (high-T decap) followed by the normal ALD-Al_2O_3 procedure without any TMA pre-dosing. Based on previous studies of InGaAs(001) with As_2 decapping and annealing at similar temperatures to those used in this research,[13,14] it is believed that the InGaAs surfaces decapped at 370 °C and 460 °C in this research form predominantly As-rich 2×4 surface reconstructions and In/Ga-rich 4×2 surface reconstructions, respectively. From Figure 1, the high-T decapped n-InGaAs sample (In/Ga-rich surface) shows larger frequency dispersion over the gate bias range from −2 V to 0 V and larger C-V stretch-out than the low-T decapped n-InGaAs (As-rich surface) capacitor, which indicates a higher density of interface defects on the high-T decapped n-InGaAs. Moreover, the minimum capacitance of the low-T decapped InGaAs capacitor measured at −2 V is 0.120 $\mu F/cm^2$, which is close to its ideal value (0.119 $\mu F/cm^2$) for 10^{17} cm^{-3} doping, but the inversion capacitance for high-T decapped InGaAs (0.147 $\mu F/cm^2$) does not reach its ideal value. This suggests that the Fermi level may be pinned between the midgap and the valence band (VB) edge of the InGaAs semiconductor,[15] which is consistent with a previous report that the Fermi level is pinned on a clean n-InGaAs(100) 4×2 surface, and that TMA dosing at 270 °C (the ALD-Al_2O_3 temperature) does not move the position of the Fermi level.[13] We can also observe that the accumulation capacitance density of the high-T decapped capacitor is slightly smaller than that of the low-T decapped sample. There are several possible reasons for this, including more efficient initiation of ALD on this surface than on the low-T decapped substrate, or possible native oxide formation on the high-T decapped InGaAs surface because of the longer exposure of the decapped InGaAs surface to the background oxidant in the ALD chamber at high temperatures during heating and cooling of the substrate.

Interface states near the conduction band (CB) edge are difficult to investigate with n-type InGaAs substrates due to the influence of border traps, which cause the frequency dispersion in accumulation[6] observed in Figs. 1(a) and 1(c). Therefore, p-type InGaAs substrates were used to characterize interface traps in the top half of the InGaAs band gap. For the p-type InGaAs MOS capacitors, while the C-V frequency dispersion for high-T decapped p-InGaAs is slightly smaller than that of low-T decapped p-InGaAs, both the high-T decapping and low-T decapping show very small dispersion at positive gate bias, indicating a relatively low density of interface defects with energies in the top half of the InGaAs band gap.

In order to investigate the effect of the large dose TMA exposure of the low-T decapped InGaAs(100) surface, 10 TMA pulses of 1 s duration (approximately 1000 Langmuir per pulse) were applied at 150 °C or 270 °C prior to the start of ~3 nm ALD Al_2O_3 deposition at 270 °C. Comparing the C-V results shown in Fig. 1(a) to those in Figs. 2(a) and 2(b), we observe that the n-type InGaAs metal-oxide-semiconductor capacitors (MOSCAPs) with TMA pre-dosing show significantly smaller frequency dispersion at negative bias and the effect of the TMA pre-dosing is independent of its temperature within experimental error. The ability of the TMA-dosed InGaAs(100) to resist subsequent oxidation[4] and to have a lower density of As-related surface defects has been noted previously.[16] Moreover, prior studies using scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) showed that As-rich InGaAs(100) 2×4 surface contains As-dimers, which bond strongly to TMA molecules. Consequently, TMA dosed 2×4 surfaces can produce a low

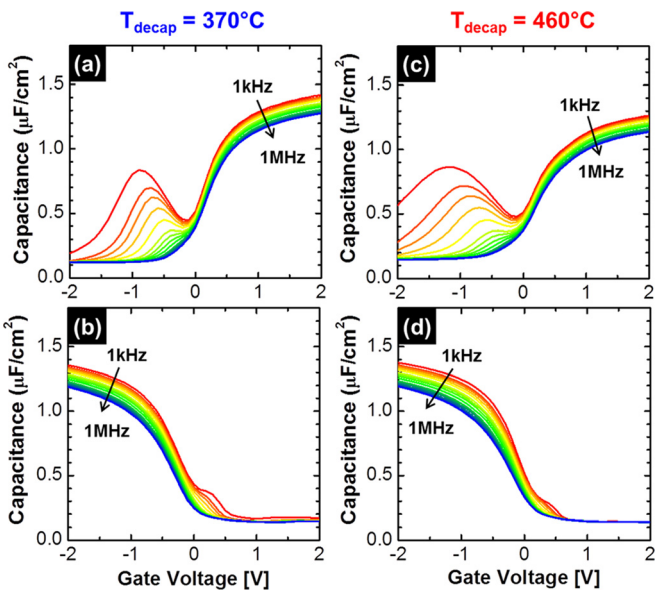

FIG. 1. Multi-frequency (1kHz ~ 1MHz) C-V curves measured from (a) n-InGaAs(100) and (b) p-InGaAs(100) MOS capacitors that were prepared by As_2-decapping at 370 °C. C-V curves from (c) n-InGaAs(100) and (d) p-InGaAs(100) decapped at 460 °C.

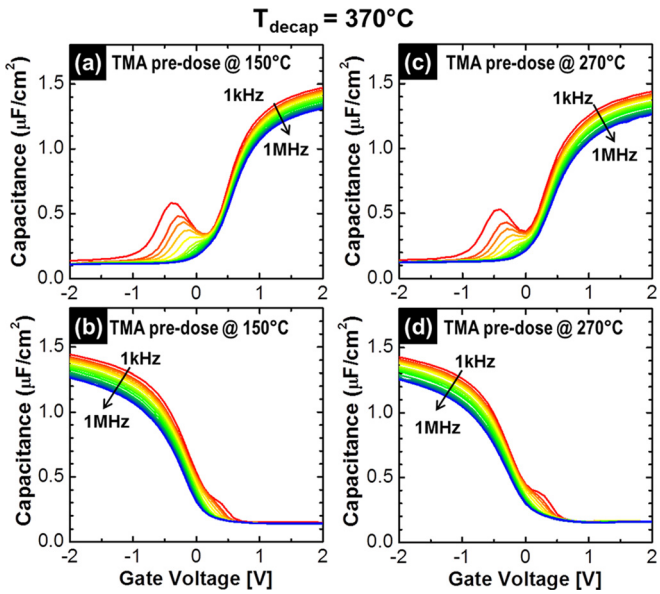

FIG. 2. C-V plots from the InGaAs decapped at 370 °C and dosed with TMA at 150 °C and 270 °C. TMA was dosed at 150 °C on (a) n-InGaAs and (b) p-InGaAs. (c) n-InGaAs and (d) p-InGaAs surfaces were treated with TMA at 270 °C.

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dangling bond density over a wide temperature range from 25 °C and 280 °C.[13] These prior STM/STS results are consistent with our C-V result showing that the effect of TMA dosing on the interface defect density appears to be temperature independent.

Interface trap densities (D_{it}) are extracted from C-V and conductance-voltage (G-V) data obtained from n-type and p-type InGaAs capacitors with and without the TMA predosing. D_{it} values are calculated by using the full interface state model with a Δ circuit of three complex elements[17] with inclusion of a series resistance for the substrate and contacts in the equivalent circuit. The n-type InGaAs samples were used to calculate D_{it} at energies in the bottom half of the InGaAs band gap and the p-type samples were used for energies at the top half of InGaAs band gap in order to avoid the influence of border traps.[6,18] Shown in Figures 3(a) and 3(b) are examples of the fits of the capacitance and conductance data as a function of the measurement frequency to the interface state model. The model for the capacitance and the conductance is in a good agreement with the experimental data.

As expected from the C-V characteristics shown in Figs. 1 and 2, the D_{it} measured from the low-T decapped InGaAs substrate (nominal 2×4 reconstruction) without pre-ALD large dose TMA exposure varies from 1×10^{13} $eV^{-1}cm^{-2}$ near the VB edge to 7×10^{11} $eV^{-1}cm^{-2}$ near the CB edge, and the estimated D_{it} after TMA predosing at 270 °C was reduced by a factor of approximately one half across the InGaAs band gap, as shown in Fig. 3(c). TMA

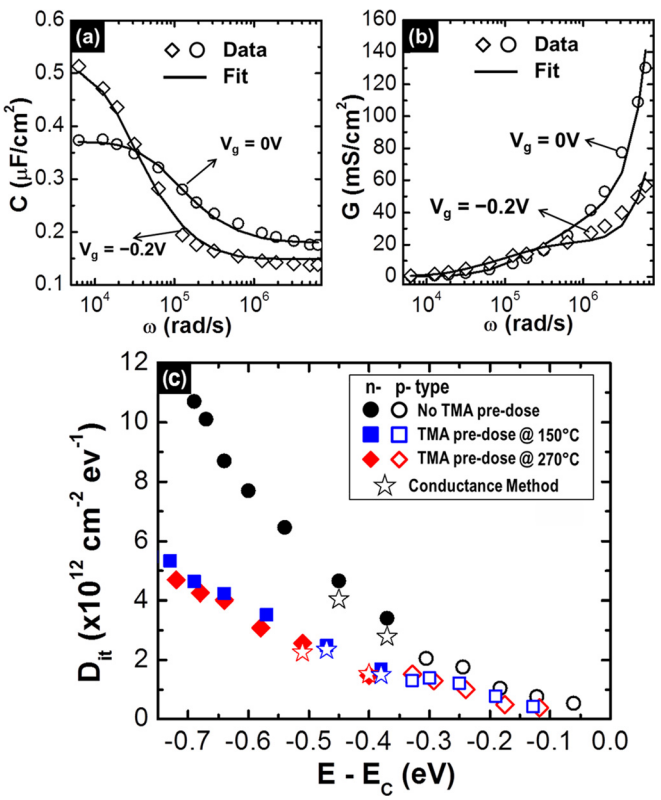

FIG. 3. Model fitting examples of (a) capacitance and (b) conductance data measured at 0 V and −2 V from a capacitor with TMA pre-dosing at 150 °C. (c) D_{it} extracted from n-InGaAs samples for the bottom half of InGaAs bandgap and from p-InGaAs samples for the top half of InGaAs bandgap.

pre-dosing at 270 °C may give a slightly lower D_{it} in the bottom half of the InGaAs band gap than does 150 °C TMA predosing, but the difference is within 10%. The observation of a peak in the C-V curves under weak inversion conditions does not correspond with a peak in D_{it} in that energy range. Instead, this C-V feature occurs because defects relatively deep in the InGaAs energy gap do not respond at room temperature even at the lowest frequencies tested in typical C-V measurements.[16]

Given the low interface trap density near the CB edge, border traps will likely limit the performance of these gate stacks, which require facile motion of the quasi-Fermi level from energies near midgap into the CB using a typical flat band device design for III-V MOSFETs.[19] D_{it} values near midgap extracted by the conductance method[20] were compared to the D_{it} values extracted with the full interface state model. The conductance method gives slightly lower D_{it} values near midgap as shown in Fig. 3(c).

In order to determine the surface bonding configuration of TMA on the As-rich $In_{0.53}Ga_{0.47}As$ (001) surface, DFT was employed to model multiple bonding geometries on the $In_{0.5}Ga_{0.5}As(001)$ 2×4 surface. All DFT simulations were performed with the Vienna *Ab-Initio* Simulation Package (VASP)[21,22] using projector augmented-wave (PAW) pseudopotentials (PP)[23] and the PBE (Perdew-Burke-Ernzerhof) exchange-correlation functional.[24,25] The choice of PBE functional and PAW PP was validated by parameterization runs demonstrating good reproducibility of experimental lattice constants, bulk moduli, and formation/cohesive energies for bulk crystalline InGaAs and its components: GaAs and InAs.

Figure 4(a) shows a side view of an ideal InGaAs(001) 2×4 unit cell containing two As-dimers on the row and one As dimer in the trough. The bonding sites and energies were determined via DFT calculations using the expected TMA dissociative chemisorption product, dimethylaluminum (DMA),[26] for three and six adsorbates, consistent with half and full coverage. For half coverage of DMA, there is only one DMA per As dimer. In contrast, for full DMA coverage, there are two DMA per dimer, so the DMA can bridge-bond between all As atoms and thereby eliminate the As dangling bonds on this surface. By having all surface As atoms bridge-bonded to DMA via As-Al-As bonds, the surface As atoms are restored to tetrahedral geometry, thereby eliminating As bond angle strain. The calculated density of states for the half and full coverage DMA is shown in Fig. 4(d).

A full coverage of surface As sites by Al is needed to avoid dangling bonds that produce D_{it} across the band gap. In general, filled dangling bonds on As atoms are one of the common causes of VB edge states and, while empty dangling bonds on group III atoms and group III homodimers are the most common cause of CB edge states, Arsenic atoms in non-tetrahedral sites can have strained bond angles which can create either VB and CB edge states. The highly strained half DMA coverage case shows a large density of midgap states and band edge states.

The DFT simulations and the C-V measurements provide a mutually consistent picture of the benefits of pre-ALD TMA dosing. A significant dose of TMA onto a clean InGaAs(100) 2×4 surface prior to the start of the ALD-Al_2O_3 can produce

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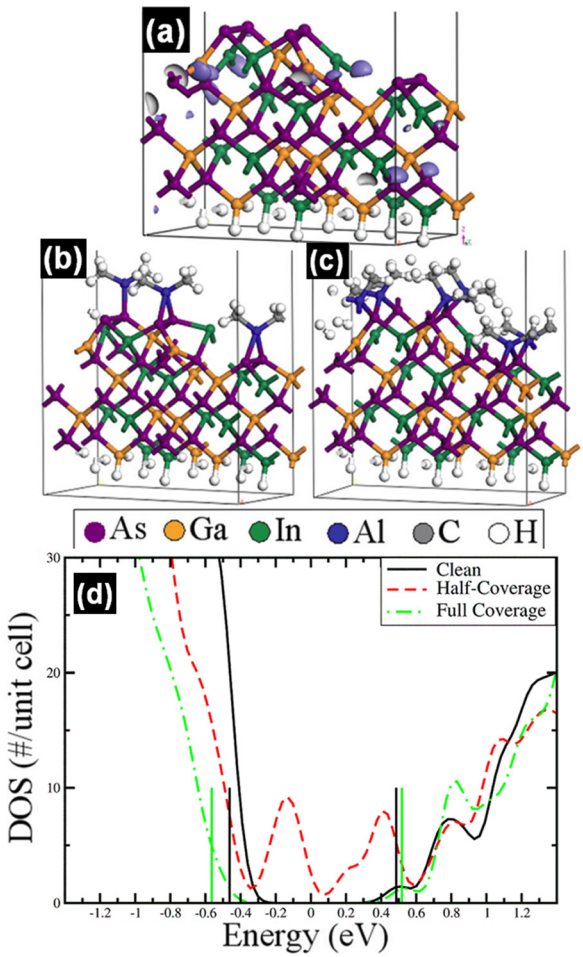

FIG. 4. DFT-MD calculations of InGaAs(001) 2×4 (a) clean surface containing a double As-dimer row, (b) half (3 DMA) and (c) full (6 DMA) coverage DMA on double As-dimer unit cell. (d) Calculated density of states. The blue lobes in (a) show the CB edge states from the clean surface are mostly on the group III surface dangling bonds. Vertical lines in (d) mark the conduction and valence band edges for the clean and full DMA coverage conditions.

a more complete DMA surface coverage, effectively passivating defect sites.

In conclusion, it has been shown that the interface properties of ALD-Al_2O_3/InGaAs(100) characterized by C-V and G-V analysis of using MOS capacitors are consistent with the InGaAs surface reconstructions reported in previous STM and STS characterization after thermal desorption of an initially present As_2 protective cap. Large-dose TMA exposure of the As_2-decapped InGaAs(100) substrate prior to Al_2O_3 ALD reduces the D_{it} distribution across the bandgap of InGaAs. These results are in agreement with DFT simulations showing that full coverage of dimethylaluminum restores surface As atoms to tetrahedral bulk-like bonding and reduces midgap states and CB edge states observed for partial coverage of the InGaAs 2×4 surface. The D_{it} distribution across the InGaAs band gap was characterized without the confounding influence of border traps by studying both n- and p-type InGaAs channels using the full interface state model. The extracted D_{it} distribution increases monotonically from the CB edge to the VB edge. Low D_{it} ($<5 \times 10^{11}\,cm^{-2}eV^{-1}$) near the CB edge is achieved by large-dose TMA exposure of the InGaAs(100) surface. These results suggest that border traps[6,18] associated with defects in the deposited oxide dielectric, rather than true interface traps, are liable to limit the performance of high-k/InGaAs MOSFETs in which the quasi-Fermi level sweeps between midgap and the InGaAs conduction band during FET operation.

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