Surface Defects and Passivation of Ge and III–V Interfaces

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Abstract

The need for high-κ gate dielectrics and metal gates in advanced integrated circuits has reopened the door to Ge and III–V compounds as potential replacements for silicon channels, offering the possibility to further increase the performances of complementary metal oxide semiconductor (CMOS) circuits, as well as adding new functionalities. Yet, a fundamental issue related to high-mobility channels in CMOS circuits is the electrical passivation of their interfaces (i.e., achieving a low density of interface defects) approaching state-of-the-art Si-based devices. Here we discuss promising approaches for the passivation of Ge and III–V compounds and highlight insights obtained by combining experimental characterization techniques with first-principles simulations.

Introduction

The success of Si-based integrated circuits relies largely on the quality of the SiO_2/(100)Si interface. The density of intrinsic defects (dangling bonds) at this interface is about 1×10^{12} cm^{-2} (References 1 and 2) and can be decreased by two orders of magnitude after annealing the devices in an N_2/H_2 atmosphere at typically 400–450°C. Such a low density of interface defects is required to fabricate metal-oxide-semiconductor (MOS) field-effect transistors with good electrical performances.

However, oxide/Ge and oxide/III–V interfaces present a much larger density of interface defects, lying in the 10^{13} cm^{-2} range,[3–7] which hampers the electrical properties of MOS devices. In the case of Ge, its oxide is known to be thermodynamically unstable at about 400–450°C,[5] making the interface defect passivation under H_2-containing atmosphere problematic. As far as III–V compounds are concerned, it is believed that their oxidation leads to the formation of a high density of intrinsic defects with energy levels in the semiconductor bandgap,[8] resulting in the so-called Fermi level pinning[3], namely the lack of modulation of the concentration of carriers at the oxide/III–V interface by the application of a gate bias.

Passivation of Ge Surfaces

Recent progress has been achieved regarding Ge surface passivation, mainly using an ultrathin Si capping layer (a few monolayers thick),[9,10] a thermally grown GeO_2 or GeON interfacial layer,[11–13] or PH_3 or H_2S surface treatments.[14,15] These interface passivation approaches have been combined with the deposition of different high-κ dielectrics, showing promising device characteristics, essentially on *p*-channel MOSFETs; most of the attempts on *n*-channel transistors resulted so far in no or barely functional devices with much lower electron mobility than expected. Recently, the passivation of Ge by its thermal oxide layer showed very promising results on *n*-channel devices.[16]

Various high-κ dielectrics have been studied as possible gate insulators for Ge channel MOSFETs.[17–21] HfO_2 (already used in commercial devices) and ZrO_2 are strong candidates for the replacement of SiO_2 in Si-based transistors. To illustrate the Ge surface passivation issue, let us first discuss the case of HfO_2 deposited by atomic layer deposition (ALD) on a hydrofluoric acid (HF)-last treated Ge surface, leaving one to two monolayers of GeO_x (about 3 to 5 Å thick) at the interface (for more on the ALD process, see the Wallace et al. article in this issue). The thickness of this interlayer is being preserved after HfO_2 deposition.[22] Note that this interfacial layer is much thinner than the typical SiO_2 interfacial layer formed during the high-temperature processing of Si devices with high-κ layers, which is typically less than 1 nm. From a scaling point of view, the HfO_2/Ge system thus presents a potential advantage over its HfO_2/Si counterpart. Unfortunately, the electrical properties of the HfO_2/Ge gate stack are quite poor,[22,23] as suggested by almost flat capacitance-voltage (*C-V*) characteristics, indicating that the Fermi level at the Ge surface is pinned at a fixed value, due to the presence of a very high density of interface states (in the 10^{13} to 10^{14} cm^{-2} range). The leakage current flowing through the gate dielectric is also very high, and the current-voltage characteristics are not reproducible from one device to the other. These poor electrical results are possibly caused by the formation of Ge–Hf bonds at the interface, as recently predicted from first-principles simulations,[24–26] as well as by the diffusion of Ge into the HfO_2 layer[22] either during the deposition or after post-deposition anneals (PDAs). Note that similar results were reported for HfO_2 layers deposited by metal–organic chemical vapor deposition (MOCVD)[22] on an HF-last cleaned Ge surface or by molecular beam epitaxy (MBE) on a clean (2×1) reconstructed Ge surface (i.e., a surface with Ge-Ge dimers that are formed in order to minimize the density of dangling bonds).[27] Proper passivation of the Ge surface is thus required before deposition of a high-κ gate dielectric layer.

Epitaxial-Si Layer Passivation

The first promising Ge surface passivation approach we will discuss consists of depositing an ultrathin Si epitaxial interlayer, followed by its (partial) chemical or thermal oxidation.[9,10,28] The advantage of this approach is that it avoids the need for Ge surface passivation and can make use of successful approaches used for Si passivation. Typically, the Ge surface is first etched in an HF solution to remove most of the native GeO_x layer. The wafer is then transferred to an epitaxial reactor, where it is baked in H_2 at a typical temperature of 600–650°C to obtain a clean Ge surface. An ultrathin Si epitaxial layer is next deposited on the Ge surface, using SiH_4 at a typical temperature of 500°C or Si_3H_8 at about 350°C. This interlayer is next partly oxidized in an O_3-based solution to form an ultrathin SiO_2 interlayer, typically 0.5 to 1.0-nm thick.

A high-resolution cross-sectional transmission electron microscope (TEM) picture

of a typical $HfO_2/SiO_x/Si/Ge$ gate stack is shown in Figure 1a.[10] A well-defined gate stack, with sharp and smooth interfaces, is observed from the TEM picture. As shown in Figure 1b, the *C-V* characteristics of a $HfO_2/SiO_2/Si/Ge$ gate stack are much improved compared to the HfO_2/Ge gate stacks with no Si passivation layers, which were almost flat. Both the high-frequency gate-to-channel capacitance (C_{gc}) and gate-to-bulk capacitance (C_{gb}) of a Si-passivated Ge-pMOSFET are well behaved (i.e., with clear capacitive responses from the minority [C_{gc}] and majority [C_{gb}] carriers), suggesting a much-improved Ge surface passivation. Consistently, the average density of interface states, estimated from charge-pumping current measurements, is about 2×10^{11} cm^{-2} near midgap.[29] The much-improved passivation of the Ge surface achieved by the epitaxial-Si (epi-Si) layer deposition allowed the fabrication of functioning pMOSFETs,[28,30] with peak hole mobilities ranging between 350–400 $cm^2\ V^{-1}\ s^{-1}$ (i.e., more than three times the typical hole mobility of Si devices).

The threshold voltage (V_{th}) of Si-passivated pMOSFETs depends on the number of Si monolayers remaining after

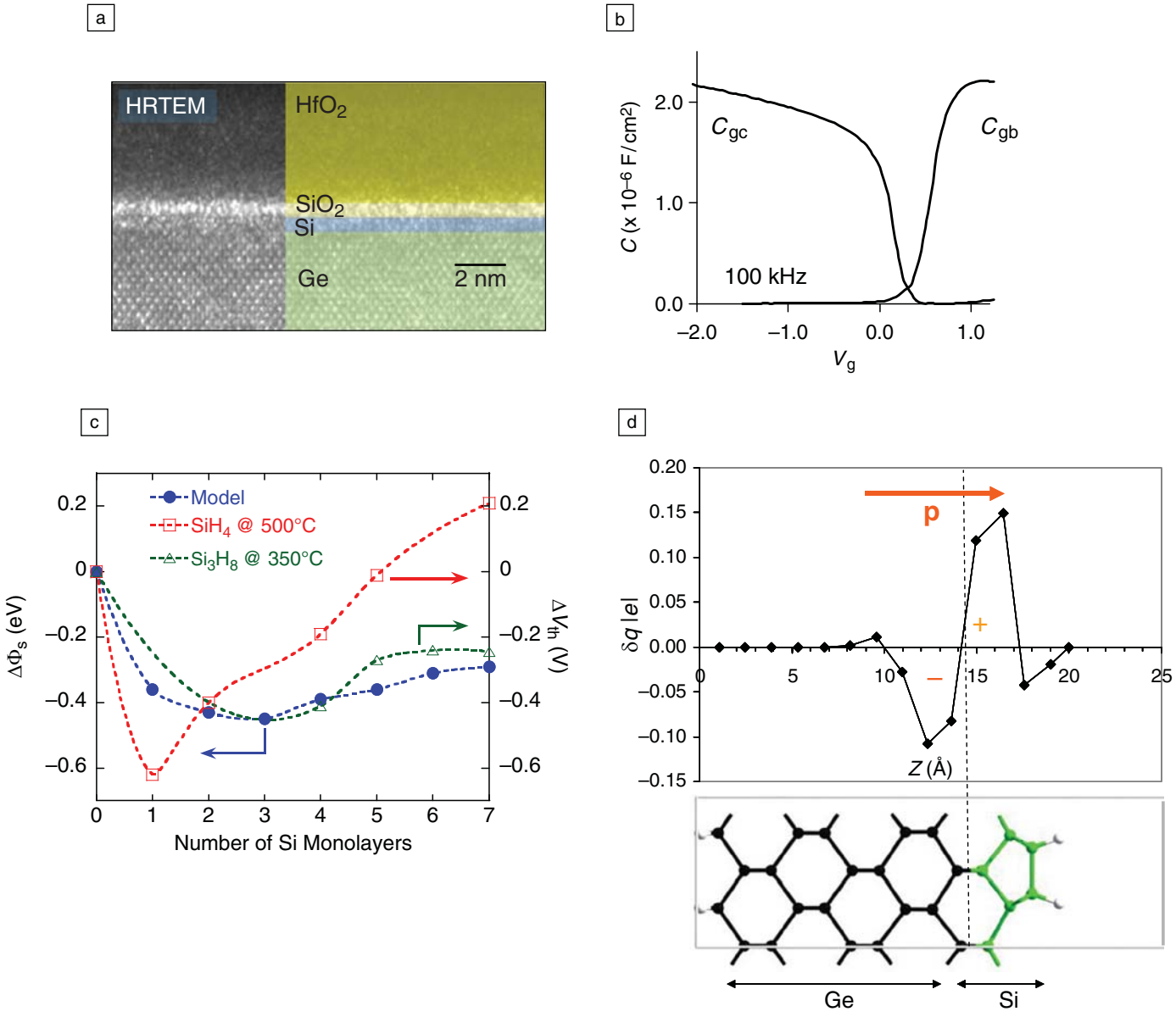

Figure 1. (a) High-resolution cross-sectional transmission electron diffraction (TEM) picture of a gate stack formed by a Ge substrate, an ultrathin epi-Si layer, partly oxidized into SiO_x, and a HfO_2 layer deposited by atomic layer deposition.[10] (b) Gate-to-channel capacitance (C_{gc}) and gate-to-bulk capacitance (C_{gb}) versus gate voltage of a Si-passivated Ge-*p*-type metal oxide semiconductor field-effect transistor, measured at 100 kHz.[10] (c) Calculated change in the work function of the Ge/Si slab ($\Delta\Phi_s$) as a function of the number of Si monolayers (MLs).[31,32] Open triangles and open squares correspond to the threshold voltage shifts measured on transistors with 350 and 500°C Si layer deposition, respectively. (d) Computed partial atomic charges δq along the Ge/Si slab (3 ML of Si)[32]; *Z* is the distance from the bottom of the slab. Black, green, and white spheres correspond to Ge, Si, and H atoms, respectively; **p**, dipole moment.

partial oxidation, as seen in Figure 1c, where the threshold voltage shift, ΔV_{th}, measured on devices with Si layers deposited at 500°C (using SiH_4) and 350°C (using Si_3H_8) are compared. In both cases, V_{th} is positive for one to four Si monolayers (i.e., the device is not turned off at zero gate bias). For Si layers deposited at 350°C, V_{th} returns to slight negative values (typically between –50 and –40 mV) with an increasing number of Si layers, while the change in V_{th} is much more pronounced for Si layers deposited at 500°C, being close to its ideal value (about –250 mV) for five Si monolayers. Part of this V_{th} shift likely arises from the formation of a dipole pointing outward from the Si/Ge surface, due to the partial transfer of electrons from Si to Ge atoms, as predicted from first-principles simulations performed on Si/Ge slabs,[31] as illustrated in Figure 1d. (More details about these calculations can be found elsewhere.)[31,32] The presence of this dipole leads to the upward shift of the electrostatic potential of the Ge/Si slab (compared to the reference Ge slab), hence to the reduction of the work function, Φ_s, of the Si-passivated surface. The computed shift in work function, $\Delta\Phi_s$, is also shown in Figure 1c. Part of this shift also comes from quantum confinement effects in the ultrathin Si layer (i.e., change in the energy bandgap of the Si layer with its thickness), resulting in changes in the valence band and conduction band offsets between Ge and Si.[31]

From Figure 1c, it appears that the simulations are in reasonable agreement with the experimental data pertaining to the Si layers deposited at 350°C. The much larger dependence of V_{th} on the number of Si monolayers deposited at a higher temperature (for four or more monolayers) suggests that defects are possibly responsible for this trend. It has been shown that Ge diffuses through the Si layer during deposition at 500°C,[29] likely producing defects that could also be responsible for the shift in V_{th} and are not accounted for in the "ideal" Si/Ge slab model. The diffusion of Ge in the Si layer is much reduced when deposited at 350°C,[30] thus reducing the density of these defects, yet still to be identified.

Passivation of Germanium with GeO_2

The passivation of Ge by its thermal oxide (GeO_2) has been revisited recently. Though GeO_2 is hygroscopic and desorbs as volatile GeO at about 430°C (in vacuum),[33] GeO_2 has been recently demonstrated to provide efficient passivation of the Ge surface.[11–13] In addition, capping the GeO_2 layer with a metal layer or with a high-κ gate dielectric provides increased robustness to GeO desorption.[16] Thermal oxidation of Ge can be performed in atomic oxygen,[34] dry O_2,[13] or in ozone. Here, results are discussed regarding the thermal oxidation of Ge in dry O_2, at temperatures typically between 350°C and 450°C, followed by *in situ* Al_2O_3, ZrO_2, or HfO_2 deposition using ALD.[13,35] A TEM picture of a typical 4 nm Al_2O_3/1.5 nm GeO_2/Ge gate stack is shown in Figure 2a, indicating a well-defined and smooth Al_2O_3/GeO_2 interface. Chemical composition analysis of the GeO_2 interlayer indicated that this layer contains mainly Ge in the +4 oxidation state.[35]

The *C-V* characteristics of Al_2O_3/GeO_2/*n*-Ge gate stacks measured at different frequencies are shown in Figure 2b. Similar curves were observed on *p*-type Ge substrates.[35] Well-behaved *C-V* curves are observed, without significant frequency dispersion in accumulation and depletion

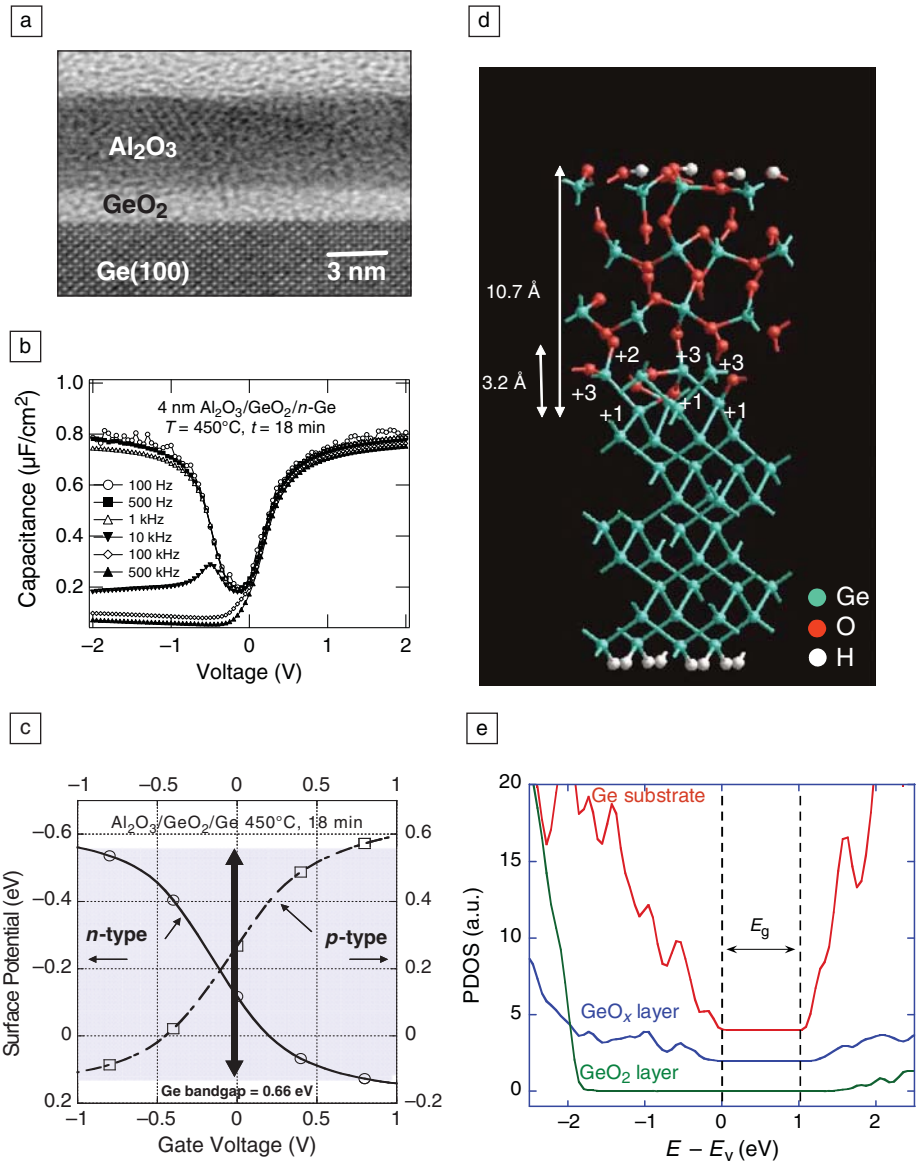

Figure 2. (a) High-resolution cross-sectional transmission electron diffraction picture of a Al_2O_3/GeO_2/Ge stack.[28] (b) Capacitance-voltage (*C-V*) characteristics of an Al_2O_3/GeO_2/*n*-Ge metal oxide semiconductor capacitor at different frequencies.[35] (c) Surface potential as a function of gate bias of Al_2O_3/GeO_2/Ge gate stacks on *n*- and *p*-type Ge substrate.[35] (d) Atomic configuration of the relaxed GeO_2/(100)Ge slab model.[24] (e) Projected electronic density of states (PDOS) of Ge, GeO_x, and GeO_2 as a function of the energy, with respect to the valence band edge E_v of Ge; E_g corresponds to the energy bandgap of the Ge slab.[24] *T*, temperature; *t*, oxidation time.

(typically between 0 and 2 V). The capacitive response of minority carriers is also observed for negative gate bias at low frequency (below 1 kHz). These *C-V* curves indicate that the interface state density, D_{it}, is low; this density was estimated by using the conductance method at low temperature[35,36] and was found to be about 1×10^{11} cm^{-2} eV^{-1} near midgap, approaching state-of-the-art Si/high-κ/metal gate devices after a N_2/H_2 post-metallization anneal (mid to high 10^{10} cm^{-2} eV^{-1}), highlighting the efficient passivation of Ge by its thermal oxide (without hydrogen PDA).

The surface potential of Al_2O_3/GeO_2/Ge stacks for *n*- and *p*-type substrates is presented in Figure 2c.[35] The surface potential characterizes the bending of the conduction and valence band in the semiconductor induced by the gate bias and is thus representative of the electric field effect (attraction of charge carriers at the semiconductor/oxide interface). The modulation of the surface potential with the gate bias indicates that the Fermi level at the surface is swept through the entire Ge bandgap (~0.66 eV) from the valence band to the conduction band (i.e., the Fermi level at the GeO_2/Ge surface is unpinned).

Interestingly, the passivation of the Ge surface by its oxide layer has been recently predicted from first-principles calculations.[24] The simulated GeO_2/(100) Ge structure, shown in Figure 2d, consists of 14 slabs of Ge layers (thickness about 18.6 Å), with the bottom Ge slab being passivated by H atoms, a ~3.2 Å thick GeO_x transition region where Ge atoms are in a +1, +2, or +3 oxidation state, a 7.5 Å GeO_2 layer where Ge atoms are in a +4 oxidation state, and about 15 Å of vacuum; this slab model, with about a 1.5 monolayer GeO_x transition region, was shown to reproduce the densities of partial Ge oxidation states observed on thermally grown GeO_2/Ge interfaces.[37] The projections of the Ge slab, GeO_x transition layer, and GeO_2 layer on the electronic density of states of the system are presented in Figure 2e. The contributions from the GeO_x transition layer and GeO_2 layer clearly lie outside the Ge energy bandgap (E_g) (i.e., the Ge–O bonds do not produce any state in the gap, regardless of the Ge oxidation state); note that the energy bandgap of the Ge slab is about 1 eV compared to 0.65 eV for bulk Ge[38,39] due to confinement effects. These findings suggest that the Ge surface should be electrically passivated by its oxide layer, consistent with the electrical data shown in Figure 2b and 2c.

Recently, well-behaved pMOSFETs with GeO_2/Ge gate stacks were demonstrated with promising characteristics.[16] Functioning nMOSFETs with similar gate stacks also were reported by the same group, with peak electron mobilities of about 270 cm^2 V^{-1} s^{-1}. These results confirm the efficient passivation of the Ge surface by its thermal oxide, provided that the desorption of the GeO_2 interlayer is suppressed during device processing.

Rare-Earth Oxides on Ge

Alternative high-κ dielectrics of HfO_2 and ZrO_2 have been investigated recently for their potential use in Ge-based MOSFETs. Among these materials, rare-earth–based oxides, such as La_2O_3[40] and CeO_2[41], have received particular attention because these oxides can be deposited directly on Ge, providing efficient passivation of the surface. The physicochemical characterization of these interfaces reveals that the deposition of these rare-earth oxides promotes the formation of a stable germanate interlayer (i.e., a mixed phase between GeO_2 and the metal oxide), likely responsible for the Ge surface passivation.[40]

To study the interaction between different metals (Al, La, or Hf) and GeO_x, which occurs at the interface between GeO_x and high-κ dielectrics[22,42] as well as in metal-oxides forming germanate layers in contact with the Ge substrate, a Ge atom was substituted by a metallic one in the GeO_x interlayer of the GeO_2/(100)Ge slab model described in the previous section.[43] The corresponding metal concentration is about 6.5 at.%. The structures obtained after geometry relaxation are shown in Figure 3a and 3b for La and Hf substitution, respectively.

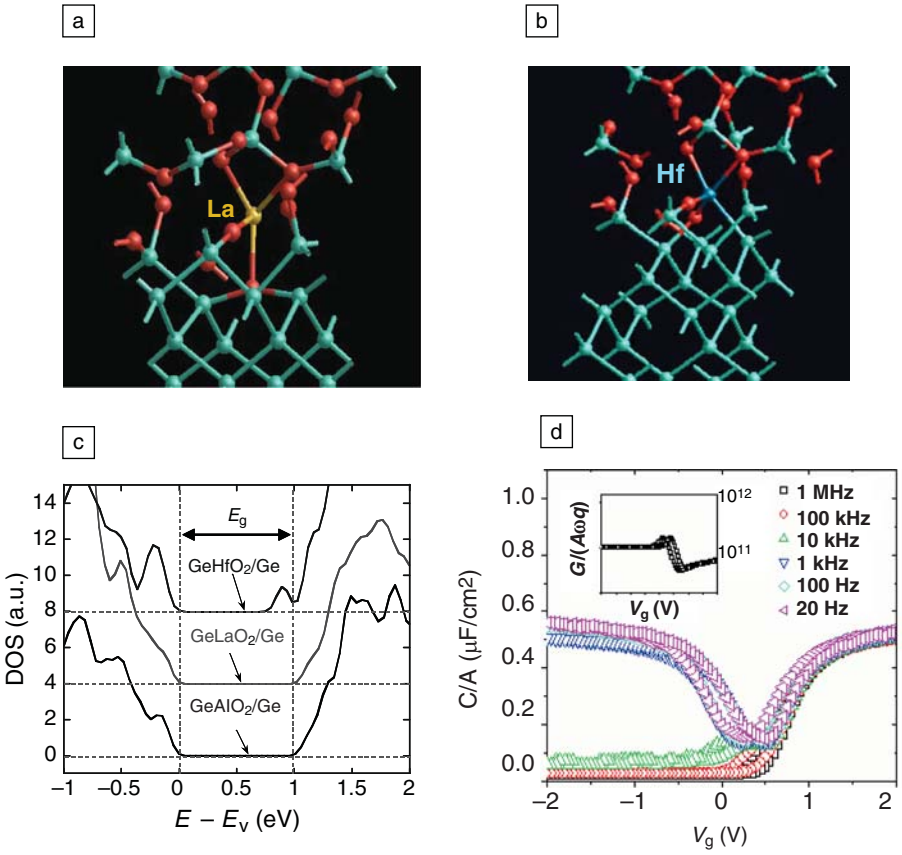

Figure 3. Atomic configurations of the relaxed Ge(M)O_2/(100)Ge structures, with a Ge atom substituted by a (a) La atom or a (b) Hf atom in the GeO_x interlayer.[43] (c) Computed electronic density of states (DOS) of the relaxed Ge(M)O_2/(100)Ge structures versus energy relative to the valence band edge (E_v) of the Ge slab; E_g corresponds to the energy bandgap of the Ge slab.[43] (d) Capacitance-voltage (*C-V*) characteristics of a Ge/La_2O_3/Pt gate stack measured at different frequencies.[40] Inset shows the normalized conductance-voltage ($G/A\omega q$) characteristics, from which a peak interface state density of about 4×10^{11} cm^{-2} is extracted. *G*, conductance; *A*, capacitor area; ω, pulsation; and *q*, electron charge.

A clear difference in behavior between Hf and La is revealed, namely Hf tends to be five-fold coordinated, whereas La (and Al) is four-fold coordinated in the GeO_x matrix. This implies the formation of an additional Hf–Ge bond at the interface,[25,26] which is not observed in the case of La and Al.[25,26] The computed electronic density of states of the relaxed structures are compared in Figure 3c. The $Ge(Hf)O_x$/(100)Ge interface presents a defect level in the upper part of the Ge energy bandgap, due to the presence of the Ge–Hf bond. The formation of this defect could explain the poor *C-V* characteristics observed on the HfO_2/GeO_x/Ge stack, discussed earlier. On the other hand, the $Ge(Al)O_x$/(100)Ge and $Ge(La)O_x$/(100)Ge structures do not present any defect level in the Ge energy bandgap, which arises from the absence of metal–germanium bonds near these interfaces.

These latter results are consistent with recent experimental data reported on La_2O_3 gate stacks deposited on clean (100) Ge surfaces by MBE, followed by a PDA in O_2 at 200°C.[40] In this study, MOS structures with Pt/La_2O_3/Ge gate stacks showed good *C-V* characteristics, with minimal frequency dispersion in accumulation and depletion (between typically 0.5 V and 2 V), indicating effective passivation of the Ge interface, as shown in Figure 3d. Interestingly, the physicochemical analysis of these stacks indicated intermixing between Ge, La, and O, likely giving rise to the formation of La-germanate layers at/near the interface.[40] These rare-earth oxides/Ge stacks also have been successfully integrated into MOSFETs, with promising electrical characteristics.[44,45]

Passivation of III–V Compound Surfaces

GaAs, InGaAs, and InAs have similar surface chemistries, which are completely distinct from that of GaN and related materials, since the latter can form highly volatile Group V oxides. Antimonides are expected to have similar surface chemistries as arsenides, but there are little data on the bonding of gate oxides to antimonide semiconductors. In this section, GaAs, InGaAs, InAs, and related materials will be referred to as the "III–As" semiconductors for brevity. This section will focus on experiments in which bonding structures have been determined by XPS, scanning tunneling microscopy (STM), and related techniques, as opposed to electrical measurements. While electrical measurements are of primary importance for device development, direct chemical information is needed to understand the passivation process.

Non-Oxide Passivation and Cleanup

To achieve a low density of interfacial defects, the III–As surface needs to be cleaned and passivated prior to deposition of a high-κ oxide. Native oxides are likely to contain suboxides, which even in the case of silicon are thought to contain a high defect density. The cleaning process is required because unlike Si and Ge, which can be cleaned by wet processing, *in situ* heating, and/or *in situ* sputter annealing, there are no similar processes that are known to leave the surface clean and well-ordered on an atomic level for GaAs, InGaAs, and related materials. Several research groups have performed a series of experiments using *in situ* XPS to characterize various wet cleaning processes, as well as the ALD cleanup process.[46–48,79,80] In wet cleaning, the III–As surfaces usually are etched in NH_4OH or $(NH_4)_2S$ to partially remove native oxides. In ALD cleanup, the wet cleaned surfaces are first exposed to the metal precursor (typically trimethyl aluminum [TMA]), which nearly reduces all the arsenic oxides and some of the Group III oxides (see the Wallace et al. article in this issue for more details).

Milojevic et al.[47] wet cleaned $In_{0.2}Ga_{0.8}As$ in $(NH_4)_2S$ prior to ALD of a-Al_2O_3 (amorphous Al_2O_3) and employed *in situ* monochromatic XPS (peak position accuracy +/− 0.05 eV) to determine the chemical shift of the interface atoms with great accuracy. TMA was employed to reduce the residual surface oxides. Since aluminum forms a stronger bond to oxygen than In, Ga, or As form to oxygen, simple thermodynamics predicts that metallic Al can reduce all of the substrate oxides. ALD reactions on III–V semiconductors are nearly always performed by first dosing the metal precursor onto the substrate until the surface is saturated with the metal precursor; at a sufficiently high temperature, this would allow the reduction of nearly all surface oxides. However, the aluminum in TMA is not metallic, and the ALD process is performed at modest temperatures (typically 300°C), where activation barriers can prevent reactions from going to completion; for example, since the heat of formation per oxygen atom is greater in Ga_2O_3 than in As_2O_5, one would expect the activation barrier for the reduction of Ga_2O_3 to be greater than that for As_2O_5. For XPS of oxide-semiconductor interfaces, the reference states of the semiconductor and oxide atoms are the bulk semiconductor and oxide atoms; for example, InGaAs would be assigned as In^{+0}, Ga^{+0}, and As^{+0}, where "+0" means bulk-like charge, whereas Al_2O_3 would be assigned as Al^{+3} and O^{-2}. XPS showed that ALD cleanup of surface arsenic oxides is effective at 300°C; post-ALD, all of the As atoms are in a As^{+0} state, consistent with As in bulk semiconductor and possible As–As bonding on the surface. However, the ALD cleanup still leaves some gallium oxides; a Ga^{+1} peak remains after ALD cleanup, consistent with either residual sulfur at the interface or Ga–O bonding.[49] The Al atoms are bulk-like Al_2O_3, consistent with Al only being in an O–Al–O bonding environment. The oxygen XPS peak shows only bonding to Al and to hydrogen from Al–OH ligands. In a recent report, Milojevic et al. employed *in situ* high-resolution XPS to examine the surface oxides during each ALD half-reaction and were able to resolve the Ga^{+1} from GaO_x and Ga–S bonding states.[48] They found that neither Ga^{+1} from GaO_x nor Ga–S are removed by ALD; conversely, they found that all arsenic sulfide species are removed by ALD. Aquirre-Tostado et al. performed a related experiment on samples for which atomic hydrogen was employed to remove native oxides instead of the NH_4S wet clean.[46] Again, a Ga^{+1} XPS peak was found at the interface, which was assigned to Ga–O bonding since no sulfur was present. This remaining Ga–O at the interface can be ascribed to either residual substrate oxides or bonding between the a-Al_2O_3 and the substrate.

a-Al_2O_3 Passivation

The ALD deposited gate oxide that has provided the best InGaAs over the past several years is Al_2O_3. For example, transistor device results from Xuan et al. for *p*-type a-Al_2O_3/InGaAs prepared by wet cleaning of the substrate show very high output current, low threshold voltages, reasonable subthreshold swings, and reasonably low off current for submicron devices.[50,51] These results and earlier related ones have catalyzed a large number of groups to investigate a-Al_2O_3/III–As MOSFETs. It is difficult to interpret electrical measurements to give direct information about atomic and molecular bonding structures such as those that can be obtained from STM and TEM. However, there are a few simple concepts that can be helpful. For III–V devices, interfacial states can be asymmetrically distributed so that the trap states can be primarily near the conduction band, midgap, or valence band. For nMOSFETs, trap states near the conduction band will reduce the output current from the ideal value, while trap states near the valence band will prevent the device from turning off and will raise the subthreshold swing from the ideal value of 60 mV/dec. In a

simple picture, trap states block full bending of the bands, thereby preventing the Fermi level from moving into the conduction band and/or valance band. However, other nontrap-related issues also can affect device performance, thereby complicating interpretation of device results; for example, poor conductivity in the source/drain regions can lower the output current, and fixed charge in the oxide can prevent the device from turning off. The issue of trap state distributions also makes a comparison between MOSFET device results and *C-V* on metal oxide semiconductor capacitors (MOSCAPs) challenging in the absence of detailed modeling.

For *p*-type $In_{0.65}Ga_{0.35}As$ 400-nm channel enhancement-mode devices prepared by wet cleaning, the following electrical characteristics have been reported: transconductance g_m (where the source drain voltage, V_{DS} = 2 V) = 350 mS/mm, threshold voltage V_T = 0.4 V, subthreshold swing, SS, = 350 mV/dec, and the ratio of the on-state to off-state current, $I_{on}(V_{GS} = 4\ V)/I_{off}(V_{GS} = 0\ V)$, = 150, where V_{GS} is the gate-source voltage.[51] The subthreshold swing is the amount of gate voltage required to increase the source-drain current by a decade and is the most direct measure of the interfacial trap state density. Although the subthreshold swing and I_{on}/I_{off} were modest, consistent with nonoptimized implanted source and drain, the output currents were high and scaled with gate length. Xuan et al. obtained better results with higher indium content devices.[50] For *p*-type $In_{0.75}Ga_{0.25}As$ 750-nm channel enhancement mode devices, g_m(extrinsic) = 430 mS/mm, V_T = 0.5 V, SS = 190 mV/dec, and $I_{on}(V_{GS} = 1\ V)/I_{off}(V_{GS} = 0\ V) = 10^6$ in the source current. Again, the modest subthreshold swing is ascribed to problems associated with the implanted source drains instead of just interface traps; therefore, there could be substantial room for improvement. Submicron devices had higher subthreshold swings consistent with this hypothesis, and the authors concluded that *C-V* analysis showed a $D_{it} = 8 \times 10^{11}/cm^2$-eV using the Terman method (high-frequency alternating current to measure the capacitance with low-frequency voltage sweep). These results may be consistent with a modest density of states at the interface throughout some of the bandgap; however, interpretation of *C-V* data at fixed temperature with just one type of doping is challenging since the Terman method does not probe the interfacial state density throughout the entire bandgap for a single type of doping at a fixed temperature. Better device results might be obtained using decapped samples and *in situ* oxide deposition after heterostructure growth since the studies cited earlier show that wet cleaning leaves some gallium oxides/sulfides, which are likely to create some interface states.

The cleanest a-Al_2O_3/$In_{0.53}Ga_{0.47}As$(100) interfaces are prepared by *in situ* decapping of As_2-capped $In_{0.53}Ga_{0.47}As$(100) followed by a-Al_2O_3 ALD.[52,53] Using this technique, McIntyre et al.[52,53] have observed a chemically abrupt interface using high-resolution TEM; high-angle annular dark field TEM also showed no interfacial oxide formation. Angle-resolved XPS spectra showed the complete absence of any chemical shift of the interfacial Ga, In, and As atoms. These XPS experiments only employed a nonmonochromatic x-ray source so a small chemical shift may still be present. In addition, variable temperature and variable frequency *C-V* measurements of $Al_2O_3/In_{0.53}Ga_{0.47}As$ stacks (*n*-type $In_{0.53}Ga_{0.47}As$) formed by *in situ* decapping indicated the Fermi level could be moved at least to midgap. Detailed modeling is required to unambiguously determine the trap density from the variable temperature variable frequency *C-V* data.[52,53]

In situ semiconductor regrowth and oxide deposition can be performed by MBE or MOCVD to provide the cleanest possible interfaces. Cheng and Fitzgerald prepared clean a-Al_2O_3/GaAs interfaces by using MOCVD to grow GaAs and a-Al_2O_3 in the same chamber.[54] TEM images revealed a completely abrupt interface, and XPS showed the absence of any arsenic oxides. Shahrjerdi et al. and Hong-Liang have observed similar TEM results for ALD-deposited a-Al_2O_3 on HF-cleaned GaAs(100).[49,55] Therefore, the comparison of interface quality must be based on XPS and electrical measurements.

Chemically, it is surprising that a-Al_2O_3 might form a low-defect density interface on III–As semiconductors because oxygen is known to pin GaAs interfaces, and it is surprising that the best interfaces show minimal chemical shift in XPS for the interfacial semiconductor substrate atoms because a-Al_2O_3 is highly ionic, so bond bonding between a-Al_2O_3 and a semiconductor should form strong bonds that induce changes in the oxidation state of the semiconductor atoms at the interface. Chagarov and Kummel have performed a series of density functional theory (DFT) molecular dynamics (MDs) simulations comparing the interface properties of a-Al_2O_3/Ge,[56] a-Al_2O_3/$In_{0.5}Ga_{0.5}As$, and a-Al_2O_3/$In_{0.5}Al_{0.5}As$/InGaAs.[57] Realistic a-Al_2O_3 samples were generated using a hybrid classical DFT MD "melt-and-quench" approach.[58] The interfaces were formed by annealing at 700 K, 800 K, or 1100 K, with subsequent cooling and relaxation (see Figure 4). The a-Al_2O_3/Ge interface demonstrates pronounced interface intermixing and interface bonding exclusively through Al–O–Ge bonds, generating high interface polarity. In contrast, the a-Al_2O_3/InGaAs interface has no intermixing, Al–As and O–In/Ga bonding, low interface polarity due to nearly compensating interface dipoles, and low substrate deformation. The a-Al_2O_3/InAlAs interface demonstrates mild intermixing, with some substrate Al atoms being adsorbed into the oxide mixed Al–As/O and O–Al/In bonding, medium interface polarity, and medium substrate deformation. The simulated results demonstrate strong correlation to experimental measurements. In simple terms, the InGaAs(100)–4 × 2 surface is very unreactive compared to Ge or InAlAs. On nearly all common InGaAs (100) reconstructions, the As atoms have filled dangling bonds, while the In/Ga atoms have empty dangling bonds; therefore, InGaAs bonds weakly to a-Al_2O_3 if the substrate is unperturbed during processing. Conversely, the Ge surface is dominated by half-filled dangling bonds, which are very reactive. InAlAs is very reactive because the substrate Al atoms make stronger bonds to oxygen than to any other substrate atoms.

Ga_2O Passivation

The use of Ga_2O_3 passivation of GaAs from an oxide source was pioneered at Bell Labs for GaAs(100).[59,60] Droopard et al. advanced the technique at Freescale Semiconductor Inc.[61,62] and developed a double source technique in which a few monolayers of oxide were deposited from a Ga_2O_3 MBE source to passivate the interface prior to deposition of GGO (gadolinium gallium oxide), which is a more fully insulating high-κ oxide. The implementation of this passivation system was nearly ideal, and the electrical properties are excellent.[63,64] A two-chamber vacuum system was employed in which GaAs wafers were regrown in one chamber and transferred in ultrahigh vacuum UHV to a separate chamber for MBE of gate oxides. This technique completely obviates the need for wet cleaning, *in situ* cleaning, or ALD cleanup. Similar techniques for *in situ* regrowth and oxide MBE under UHV conditions are currently being pursued by the University of Glasgow,[65] University of California, Santa Barbara,[81] and National Tsing Hua University.[66] The passivation layer formed by Ga_2O_3 MBE has been characterized by STM, XPS, reflection high-energy electron diffraction

(RHEED), photoluminescence, as well as electrical measurements (*C-V*, *I-V*).

The Ga_2O_3 passivation was performed on *in situ* regrown wafers so the surfaces were clean and well characterized. The surface layers were the As-rich reconstruction of GaAs(100)–2 × 4. This surface is dominated by the β2 reconstruction, which consists of pairs of As dimers. The passivation layer was formed by MBE deposition of gallium oxide from a Ga_2O_3 source. Ga_2O_3(s) evaporates as Ga_2O(g) + O_2(g), but Ga_2O(g) has a high sticking probability, while O_2(g) has a low sticking probability. Using *in situ* RHEED, Droopad et al. showed that Ga_2O formed an ordered monolayer as the RHEED switched from the clean surface 2 × 4 to a c(4 × 2) reconstruction.[62] Using STM, Hale et al. showed that initially, the Ga_2O inserts into the As double dimers.[67] Using XPS, Droopad et al. showed that no As–O bonds were formed consistent with the STM imaging.[62] The XPS also showed that Ga was only in either the substrate Ga^{+0} state or in the oxide Ga^{+3} state. Scanning tunneling spectroscopy (STS) experiments showed that the Ga_2O bonding to the As dimers leaves the Fermi level unpinned, while DFT modeling shows that good electrical properties are due to Ga_2O restoring the surface As atoms to a more bulk-like charge state (see Figure 5).[68] For example, the most stable bonding structure is an insertion of Ga_2O into row dimers that replace As–As dimer bonds with bulk-like As–Ga bonds. Since Ga_2O_3 is a poor insulator, practical MOSCAPs and MOSFETs are always fabricated by depositing a GdGaO layer on top of the gallium oxide passivation layer. Recently, improvements have been made in the source drain contacts for buried channel $In_{0.3}Ga_{0.7}As$ channel MOSFETs, which have been fabricated by Hill et al. with this passivation system.[65] A capping/barrier layer of GaAs was employed; therefore, the key passivation interface was Ga_2O/GaAs(100)–2 × 4. This provided subthreshold swings of 102 mV/dec and mobilities measured with an *I–V* of 5500 cm^2/Vs along with g_m(extrinsic) = 475 μS/μm and I_{on}/I_{off} ~10^7 for 1-μm devices. With identical on-state parameters, subthreshold swings of 65 mV were recently reported, and transistor performance was shown to match ideal models.[69]

The Ga_2O_3/GGO MOSFET has a surface layer of GaAs(100)–2 × 4, and it may be hard to extend this passivation system to higher indium content devices. Higher indium content InGaAs semiconductors have different real space 2 × 4 reconstructions than GaAs(100), and any indium incorporation into the oxide during processing could be problematic since indium oxides are often poor insulators. The temperature process windows for this passivation system is narrow, so extension beyond GaAs may be challenging. For example, Hill et al. fabricated $In_{0.75}Ga_{0.25}As$ channel MOSFETs with a $In_{0.53}Ga_{0.47}As$(100) capping layer using an oxide stack similar to Ga_2O_3/GGO.[65,70,71]

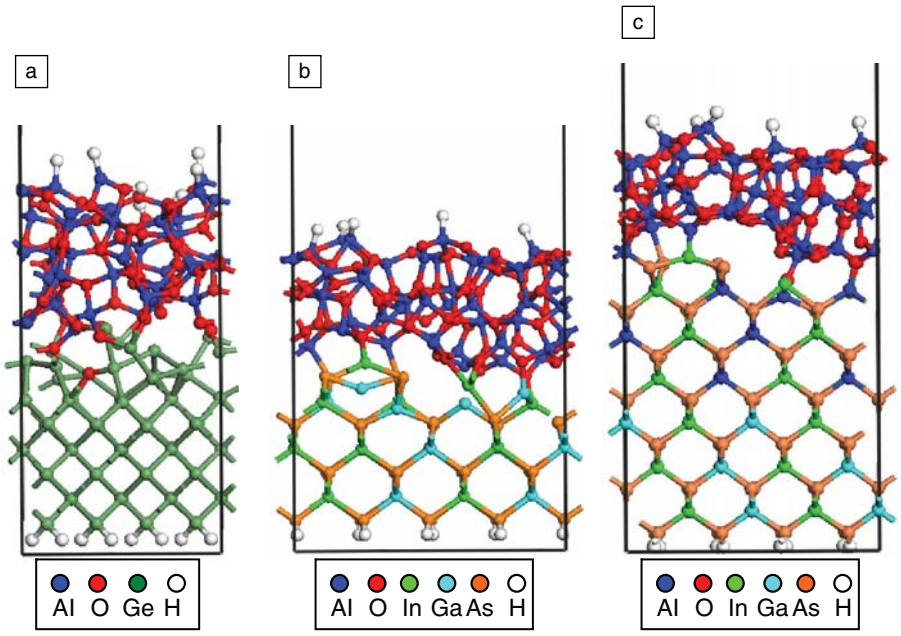

Figure 4. Density functional theory simulation of amorphous a-Al_2O_3-semiconductor interface bonding structures.[56,57] (a) 700 K annealed a-Al_2O_3/Ge(100)–2 × 1: Al atoms migrate out of interface; O atoms migrate into the interface; in the final systems, all the oxide semi-bonds are Al–O–Ge. Density of states (DOS) shows oxide-induced states near the Fermi level. (b) 800 K annealed a-Al_2O_3/Ge(100)–2 × 1. Final structure has polar As–Al bonds and O–In/Ga bonds of opposite dipole direction, small displacement of InGaAs atoms, and low InGaAs lattice distortion. DOS shows no midgap states, but the Fermi level is in the conduction band, consistent with a small dipole at one of the interfaces. (c) 800 K annealed a-Al_2O_3/Ge(100)–2 × 1. During annealing, Al migrated from InAlAs to Al_2O_3, resulting in interfacial mixing. DOS shows a high density of midgap states.

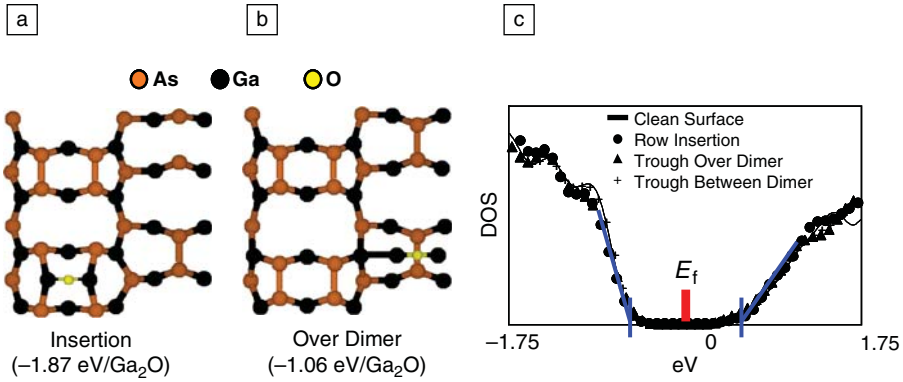

Figure 5. Density of states (DOS) modeling of the passivation of GaAs(100)–2 × 4 by Ga_2O.[68] (a) Bonding of Ga_2O to the As–As row dimers through insertion into a pair of dimers. This is the most stable site and the one observed readily at low coverage in scanning tunneling microscopy (STM). (b) Bonding of Ga_2O in the trough by bonding over the trough As–As dimers. The trough is observed to fill at high coverage in STM. (c) Density functional theory calculations of the DOS show that all the Ga_2O sites leave the bandgap free of states consistent with an unpinned Fermi level (E_f).

While very high output currents were measured (g_m = 737 μS/μm) for a 1-μm gate length, a large negative threshold voltage was observed, which was attributed to trap states. Preliminary STM/STS work by Shen et al. shows that submonolayers and monolayers of In_2O on In/Ga-rich InGaAs(100)–2 × 4 leave the surface unpinned,[72] but no oxide stack data are available. Even though the GGO/Ga_2O_3/GaAs(100)–2 × 4 passivation system has not yet been as successful on InGaAs, it provides a clear model of one type of successful passivation system: ordered covalent bonding of a monolayer of suboxide that not only maintains the substrate atoms in the clean surface positions but restores the substrate atoms to a more bulk-like charge environment.

Silicon Passivation

Silicon has been investigated as a passivation material for III–As semiconductors for over two decades.[73,74] Recently, Kambhampati et al. and Oktyabrsky et al. have extensively investigated the use of 1–3-nm thick amorphous silicon (a-Si) passivation layers between III–As semiconductors and HfO_2 gate oxides.[75,76] The a-Si layer is deposited by physical evaporation typically at <100°C substrate temperature. The goal of the a-Si layer is to prevent oxidation of the semiconductor substrate during gate oxide deposition or exposure to ambient for *ex situ* gate deposition; the silicon might also prevent intermixing or ionic bond formation.

Kambhampati et al. have shown that the a-Si passivation layer can be reduced to 0.25 nm using a fully *in situ* process for $In_{0.2}Ga_{0.8}As$, where the HfO_2 oxide is deposited on the a-Si without exposure to ambient.[75] Kambhampati et al. compared the electrical properties of *n*-type and *p*-type GaAs and $In_{0.2}Ga_{0.8}As$ MOSCAP as well as GaAs MOSFET with a-Si passivation of varying thickness. The a-Si was grown at 300 K, while the HfO_2 was grown by Hf e-beam evaporation in an O_2 ambient. The MOSCAPs had a 600°C PDA in N_2, while the MOSCAPs' implanted source drains were activated at 750°C, which resulted in nanocrystalline HfO_2, as shown by TEM. Angle-resolved XPS showed that a-Si is partially oxidized during HfO_2 deposition and contains arsenic. Angle-resolved XPS showed that Si prevents formation of AsO_x during oxide deposition; however, there are extensive $AsSiO_x$ components consistent with residual background As deposition during Si deposition as opposed to interfacial mixing. This is partially the result of experimental conditions since the Si deposition was performed in a III–V MBE chamber. *C-V* measurements show that a-Si passivation greatly reduced the *C-V* stretch out for these HfO_2/GaAs MOSCAPs, even for a 0.5-nm thickness on GaAs and a 0.25-nm thickness on $In_{0.2}Ga_{0.8}As$. For the GaAs MOSFET, a thicker 1.5-nm a-Si layer was employed, probably due to the higher temperature PDA required for implant activation. Oktyabrsky et al.[76] showed that if the silicon is not fully oxidized, it can act as a dopant source to the channel for annealing temperatures above 700°C. It is noted that the a-Si passivation layer may be more effective with ALD gate oxide because the precursors are less reactive than e-beam-deposited metals, and ALD is performed at modest temperatures.[76]

In a subsequent paper, Koveshnikov et al.[77] reported nearly as good electrical results for $ZrO_2/In_{0.53}Ga_{0.47}As$ MOSFETs with a buried channel but without the a-Si layer and with a reduced PDA temperature of 600°C.[77] However, the basic concept of a sacrificial passivation layer to protect the substrate during oxide processing is extremely valuable, because it shows that even if an oxide-semiconductor interface is stable under operating conditions, defects can be introduced during oxide processing, which creates trap states; this process-induced trap formation can be prevented by passivation.

Summary

Recent progress in Ge and III–V surface passivation has been reviewed in this article. For Ge, a few passivation approaches have been successfully developed, including the deposition of a very thin epitaxial Si layer, the thermal oxidation of Ge, and the deposition of rare-earth oxides on clean Ge surfaces. All of these approaches allow for the fabrication of functioning pMOSFETs (metal oxide semiconductor field-effect transistors), with peak hole mobilities exceeding those of reference SiO_2/Si interfaces by a factor of two to three. Though some reports also have demonstrated functioning nMOSFETs with excellent electron mobilities, especially for Ge/GeO_2-passivated interfaces, most of the results reported in the literature indicate poor nFET performances. This could be related to a fundamental issue (i.e., the charge neutrality level of Ge lying close to the valence band edge), which makes it difficult to form an electron channel at the surface,[78] or related to an asymmetric distribution of interface states in the Ge bandgap, with a very high density of interface states (up to 10^{13} cm^{-2} eV^{-1}) near the Ge conduction band edge.

The lack of high-performance Ge-nFETs requires the development of III–V compound-based devices for the fabrication of complementary MOS circuits. In that respect, the highest current III–V MOSFETs fabricated so far with ALD have all employed a-Al_2O_3, but it is possible that other oxides might also form good interfaces by ALD with the following conditions. (1) The metal precursor cannot disrupt the substrate during deposition. Trimethyl aluminum (TMA) is a particularly good precursor, since the methyl groups bind very weakly to GaV substrates. (2) The oxide has to be resistant to atom donation to/from the substrate. Due to the very strong bonding in a-Al_2O_3, the Al and O atoms are unlikely to either incorporate into the substrate or to pull substrate atoms into the oxide unless the substrate contains Al. Even a small amount of interfacial reactions can pin the interface by generating As atoms with dangling bonds. (3) The oxide needs to bond weakly to the interface or to form nearly covalent bonds to the interface. Because a-Al_2O_3 has sufficiently strong internal bonds and a narrow range of coordination numbers, it only bonds weakly to the substrate. This removes the issue of strong ionic bond significantly disturbing the electronic structure of the interface. Other strategies of forming passive interfaces on III–V surfaces rely on covalent bond formation.

On the other hand, the highest current III–V MOSFET fabricated with MBE oxide has employed Ga_2O_3/GGO or a similar oxide stack. The oxide-semiconductor bonding is very different for Ga_2O versus a-Al_2O_3 passivation: (1) the MBE Ga_2O passivation layer (passivation layer = the first oxide layer) is ordered, while the ALD a-Al_2O_3 passivation layer is amorphous; (2) the MBE Ga_2O passivation layer bonding to GaAs is strong, but DFT calculations and XPS show it restores the surface atoms to a bulk-like charge state; (3) the ALD a-Al_2O_3 passivation layer bonding to InGaAs is weak according to DFT, and XPS and DFT show it leaves the substrate atoms in a nearly bulk-like charge state. In sum, two very different oxide-semiconductor bonding schemes can provide good interfaces, but both share two key common features: restoring bulk-like charge and preventing substrate atom displacement.

The recent progress achieved in the passivation of Ge and III–V surfaces, in combination with high-κ gate stacks, are very promising for the possible co-integration of these high-mobility channels into 16 nm and beyond CMOS generations. Though much effort is still needed in order to fundamentally understand their surface passivation (further boosting device per-

formances and integrating Ge and III–V compounds on large Si substrates), these high-mobility channels should help in fabricating very high-performing IC circuits, with added functionalities and drastic reduction in power supply and power consumption, and in opening the door to "green" IC technology.

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