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# Atomic Imaging of Atomic H Cleaning of InGaAs and InP for ALD

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Air exposed III-V surfaces nearly always have electronic defects which prevent full modulation of the Fermi level thereby impeding their use in practical semiconductor devices such as metal oxide field effect transistors (MOSFETs). For a high speed device, the air induced defects and contaminants need to be removed to reduce trap states while maintaining an atomically flat surface to minimize interface scattering thereby maintaining a high carrier mobility. Using in-situ atomic scaling imaging with scanning tunneling microscopy, a combination of atomic H dosing, annealing and trimethyl aluminum dosing is observed to produce an ordered passivation layer on air exposed InGaAs(001)-(4×2) surface with only monatomic steps. A similar atomic H cleaning procedure has been demonstrated to produced an ordered passivation layer on air exposed InP(100).

## Introduction

Several hundred research papers are published each year upon development of MOSFETs using III-V semiconductors, especially InGaAs [1]. To enable low power MOSFET operation, a low supply voltage is required, the semiconductor must have high mobility and high saturation velocity, the oxide-semiconductor interface must have a low density of trap states ($D_{it}$), and the oxide-semiconductor interface must be nearly atomically flat. Surface channel III-V MOS devices can be fabricated with atomic layer deposition (ALD) high-K gate-first processes [2-5] which are similar to silicon processes for $SiO_2$ growth on silicon or ALD of high-K on silicon [6-10]. For silicon, the only commercial ALD high-k fabrication process is a replacement gate process (a type of gate last process) to avoid processing induced damage [11]. By using a gate-last process, the dielectric and oxide/semiconductor interface can avoid major damage from processing; however, the key to a gate-last process is the condition of the III-V channel prior to dielectric deposition. It has been shown that ALD of trimethyl aluminum (TMA) [12, 13] or tetrakis(ethylmethylamino)hafnium (TEMAH) [14] on III-V has self-cleaning properties by reducing the presence of As-O and Ga-O bonds. However, for high quality dielectric semiconductor interfaces, further reduction or cleaning may be required and the interface

must be atomically flat. Furthermore, aggressive oxide thickness reduction (EOT scaling) is needed to fabricate small gate length devices with small subthreshold swings, and aggressive EOT scaling requires a very high uniform ALD nucleation density with no pinholes due to surface contaminants [15]. The key barrier to a very practical problem is a simple surface chemistry challenge: development of a chemical process, which removes all air induced defects and contaminants and leaves the III-V surface flat and electrically active for high nucleation density ALD gate oxide deposition which unpins the Fermi level.

While InGaAs(100) is the most common channel material for high mobility channels, InP(100) has been used successfully as a capping layer on the narrower bandgap InGaAs(100) channel. By using the InP layer, the energy level of the defects can be controlled. However, minimal trap and fixed charge density at the oxide/InP(100) interface are still critical issues. The purpose of comparing InP to InGaAs is motivated by recent results using an InP layer on scaled MOSFETs [16, 17]. The wide bandgap layer might influence the energy levels of the density of interface trap states ($D_{it}$) loacted at the oxide/semiconductor interface and their impact on the on and off currents. If the $D_{it}$ of the dielectric/InP interface moves higher towards the conduction band edge of the InP capping layer and away from the energy levels in the InGaAs bandgap over which the Fermi level is modulated, an improvement in device performance may occur. For InP, the Fermi level pinning position is usually 0.12eV below the conduction band edge [18]. The InP layer may also act as an electrostatic control layer which would confine carriers in the channel, and the mobility of the carriers might improve by decreasing surface scattering. The surface scattering in the channel with an oxide/InP/InGaAs stack should be better than for a simple surface channel oxide/InGaAs stack because the latticed matched $In_{0.53}Ga_{0.47}As$ and InP should produce a well ordered interface with low surface roughness in comparison to an InGaAs/oxide interface.

Atomic H cleaning of GaAs, InGaAs, and related semiconductors has been investigated [19-26]. Traditional atomic H cleaning is performed at elevated temperatures as surface preparation for molecular beam epitaxial growth. Atomic H cleaning of InP has also been studied by many group using RHEED [27, 28], and XPS [26, 29, 30]. This study investigates the atomic H cleaning at 380ºC with post cleaning annealing to determine the influences of cleaning and annealing temperature on electronic structure as well as surface defects, roughness, and step density. This is in contrast to previous works which did not study the influence of post cleaning annealing. These post cleaning annealing studies are enabled use of in-situ atomic structure characterization using scanning tunneling microscopy (STM). Atomic H has been shown to unpin GaAs [24]; however, it induces surface etching [23, 31, 32]. Previous STM studies of atomic H cleaning of GaAs(100) showed there was a high step density which could be reduced by annealing in an $As_2$ flux [25]; while an excellent solution for MBE growth of quantum wells, this technique would be difficult to implement in an ALD tool. For GaAs, the atomic H etch rate increases with temperature as well as pressure of atomic H [33]. Etching must be minimized since it can induce surface roughness, which is incompatible with the thin channel structures required in low power highly scaled devices [10, 34, 35]. By employing STM of atomic H cleaned surfaces, the surface features can be studied at the atomic level.

In the present study, the InGaAs samples are 0.2μm thick $In_{0.53}Ga_{0.47}As$ layer grown by MBE on commercially available InP wafers. The MBE-grown InGaAs layers are doped *n*-type and *p*-type with a doping concentration of $2\times10^{18}$ $cm^{-3}$ of Si and Be dopants. Following MBE growth, all samples are capped with a 50nm $As_2$ layer and shipped/stored under vacuum before being loaded into the UHV chamber. The $As_2$ capped samples allow for comparison of pristine samples to air exposed/H cleaned samples. A diagram of the system chamber can be seen in Figure 1.

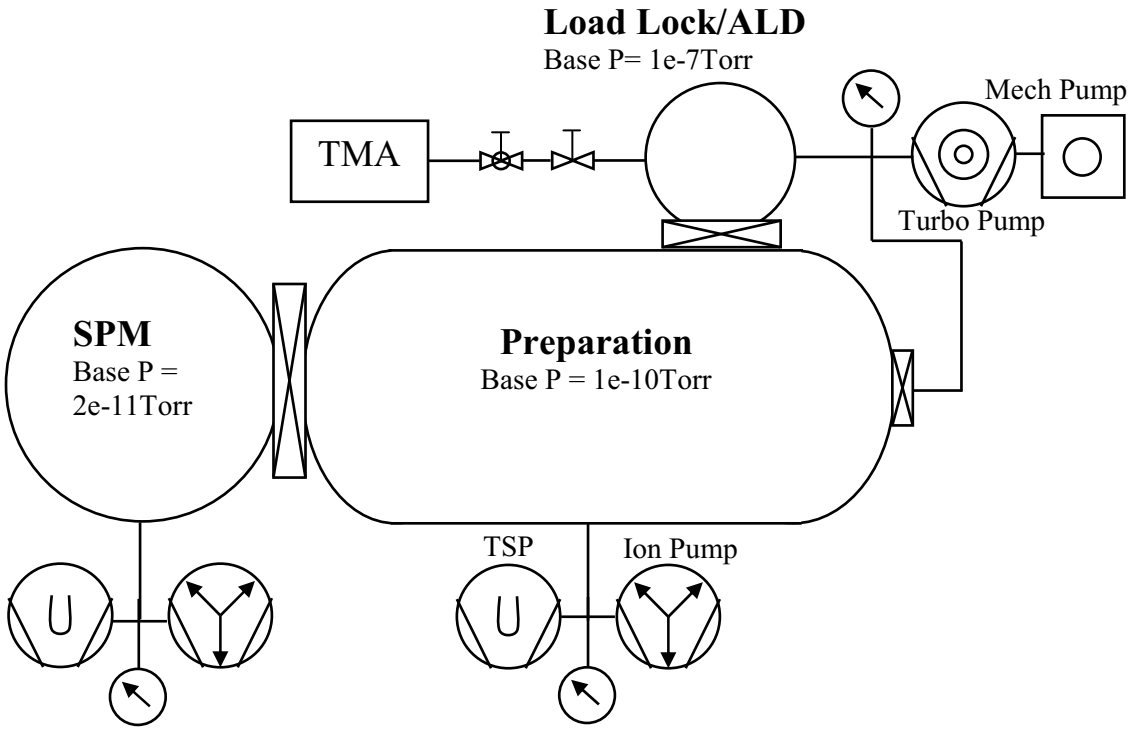



Figure 1: Diagram of ultra high-vacuum (UHV) system chamber. The scanning probe microscopy (SPM) chamber has base pressure $2x10^{-11}$ Torr. The SPM chamber contains an Omicron STM/AFM VT capable of performing STM, STS, atomic force microscopy (AFM), Kelvin probe force microscopy (KPFM). The preparation chamber has base of $1x10^{-10}$ Torr, and the atomic H cracker is located in the preparation chamber. The preparation chamber also contains a dual anode x-ray photoelectron source and analyzer, mass spectrometer, tip cracker, and low energy electron diffraction (LEED). The load lock is pumped by a turbomolecular pump to achieve a base pressure of 1 x $10^{-7}$ torr; the turbomolecular pump is also used to remove any residual water in the load lock that might react with the TMA.

The InGaAs samples are loaded into an Omicron UHV chamber with base pressure below $1x10^{-10}$ Torr. Samples are decapped in UHV and annealed at 450-470 ºC to form the InGaAs(001)-(4×2) surface reconstruction in the preparation chamber. Further details concerning the samples and preparation methods are published in reference [36]. Once the decapped surface structure is confirmed with STM in the scanning probe microscopy (SPM) chamber with a base pressure of $2x10^{-11}$ Torr, the decapped sample is transferred to the load lock and exposed to air for 0.5-30 minutes. Using an Oxford Applied Research TC-50 thermal gas cracker in the preparation chamber, the sample is cleaned with atomic H at various sample temperatures and dose times with a $H_2$ pressure of $1\text{-}2x10^{-6}$ Torr. The percent of atomic H from the thermal

cracker at 65 watts is ~50%, and the thermal cracker was operated at 60 watts. The flux of all gas at the sample surface is a mixture of the recombined background $H_2$ and the stream of atomic H from the thermal cracker. The background $H_2$ should be inert; therefore, the reduction in surface oxides is from the atomic H produced with the thermal cracker; however, the exact dose of atomic H is unknown. Therefore, each hydrogen source and dosing system will have different fluxes and require calibration to the dosing times reported in this manuscript. Following the atomic H cleaning, the sample is annealed to 460-480 ºC to regain the InGaAs(001)-(4×2) surface reconstruction, and STM is employed to determine the reconstruction, defect density, and surface roughness. The TC-50 thermal cracker employs a hot iridium tube to crack the $H_2$ molecules thereby avoiding contamination that can occur with hot tungsten filaments and or formation of ions that can occur with a plasma source; both metal contamination and ion bombardment are likely to negatively influence surface cleaning, ordering, and electronic passivation. The deposition of TMA is performed in the load lock. Prior to ALD dosing, the load lock is baked over night until it reaches a base pressure below $1x10^{-7}$ Torr to avoid water contamination (commercial ALD tools employ hot walls, which is a similar but faster technique). The sample is exposed to $1x10^{-3}$ -$1x10^{-2}$ Torr of TMA vapor for 5 seconds at room temperature (RT) followed by a 250 ºC anneal in the preparation chamber

A similar sample procedure was used for the InP samples. The InP samples employed in this study are from an InP wafer with 1μm of InGaAs channel layer doped with $4\times10^{18}$ $cm^{-3}$ of Si channel layer and a 2nm InP undoped surface top layer. The samples were first degassed for several hours at 150 ºC, followed with an exposure of atomic H to remove the oxide. The surface was inspected with STM to determine the quality of the cleaned surface. A comparison to a decapped surface was not performed because InP does not have an equivalent capping and decapping method used for the InGaAs. The goal is to use the same surface preparation from InGaAs on InP to prepare the surface for an ALD gate oxide deposition. After atomic H cleaning, the InP surface was exposed to $1x10^{-3}$ -$1x10^{-2}$ Torr of TMA vapor for 5 seconds at room temperature (RT) followed by a 250 ºC anneal in the preparation chamber.

## Results and Discussion

InGaAs(100): Figure 2(a) shows the STM image of the decapped InGaAs(001)-(4×2) surface. The decapped surface includes two distinct defects: dark horizontal features (black rectangle) and bright vertical features (white rectangle). After the InGaAs(001)-(4×2) surface is exposed to air for 0.5 minutes, an amorphous film is observed by STM, Figure 2(b). Note the surface was annealed to 200 ºC in order to achieve stable STM images. This oxide film should consist of primarily $As_2O_3$, $Ga_2O_3$, and $In_2O_3$ [20]. Figure 2(c) shows a surface exposed to air for 30 minutes followed immediately by atomic H cleaning at 380 ºC for 30 minutes. The atomic H cleaned surface shows dark features (red rectangle) consistent with monolayer etch pits; however, there is a reduction in the other defects observed on the decapped surface. Figure 2(d) shows the atomic H cleaned surface after an anneal of 460-480 ºC for 10 minutes showing an increase in terrace size and uniformity. The densities of horizontal dark defects (black rectangle) appear to be similar to the decapped surface while the vertical defects are drastically reduced. There are some bright vertical features, but the structures appear different from the features on the initial decapped surfaces.

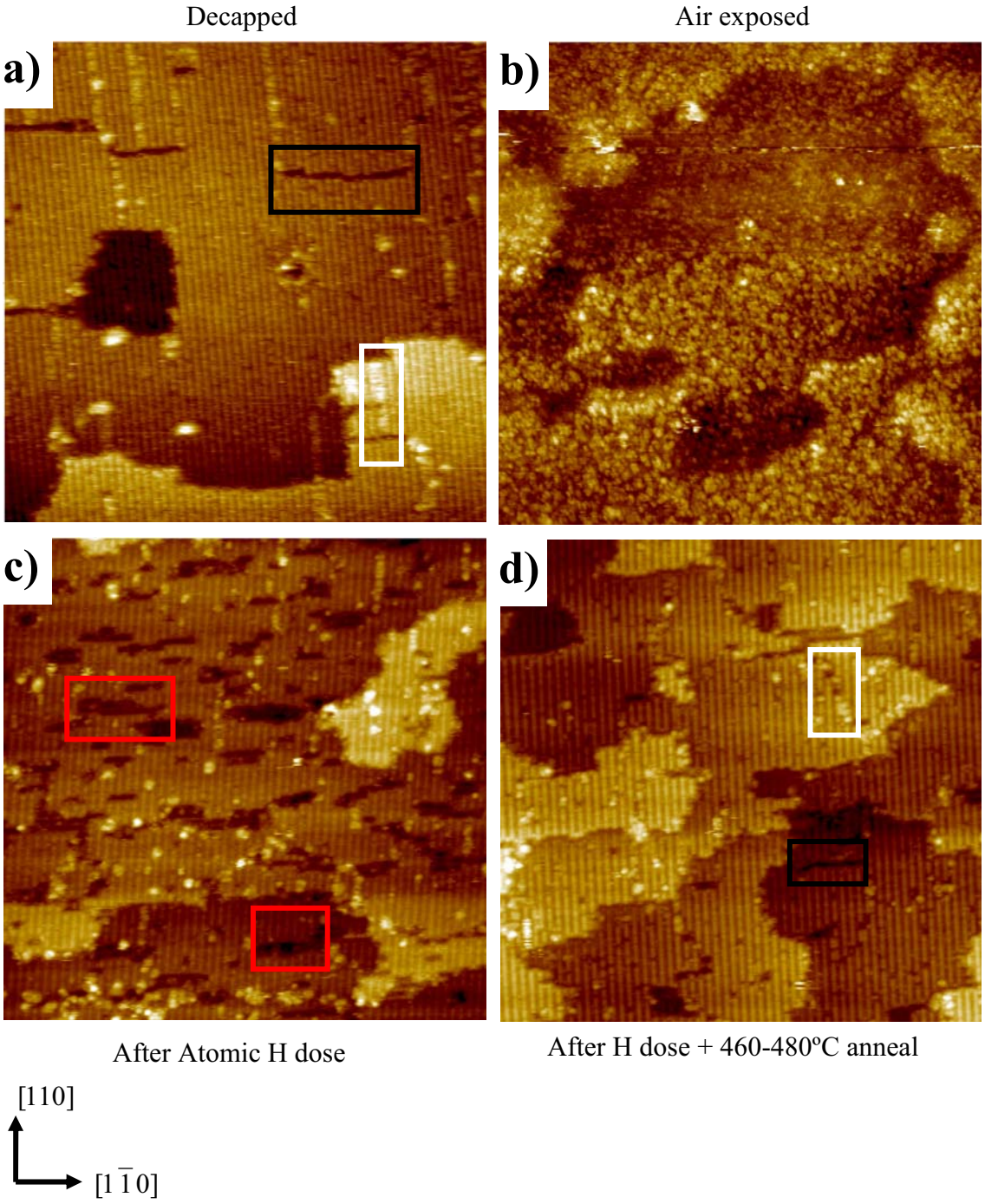



Figure 2: 100×100nm$^2$ filled state STM image of InGaAs a) decapped surface, b) air exposed and annealed to 200 ºC surface, c) surface after 30 minutes air exposure followed by 30 minutes dose of atomic H at 380 ºC, and d) surface after 30 minutes air exposure, 30 minutes dose of atomic H at 380 ºC, and a high temperature anneal to 460-480 ºC. The black rectangles show dark horizontal defect features, white rectangles indicate vertical bright defect features and red rectangles show dark surface features seen after atomic H dosing which might be from surface etching. After annealing to 460-480 ºC, the surface contains fewer dark horizontal defects and bright vertical defects.

Figure 3(a) is an STM image of the decapped surface showing ~242 (manually counted) of the bright vertical defect features with large terraces. After exposure to air

for 30 minutes and a 30 minute dose of atomic H at 400 ºC, the number of bright vertical defects is reduced to ~70 in Figure 3(b); however, the STM image shows reduction in terrace size because of the dark monolayer deep etch features. Finally, if the sample is annealed to 460-480 ºC the bright features are further reduced to ~50 in Figure 3(c), and the terrace size is restored to almost the same size as the decapped surface.

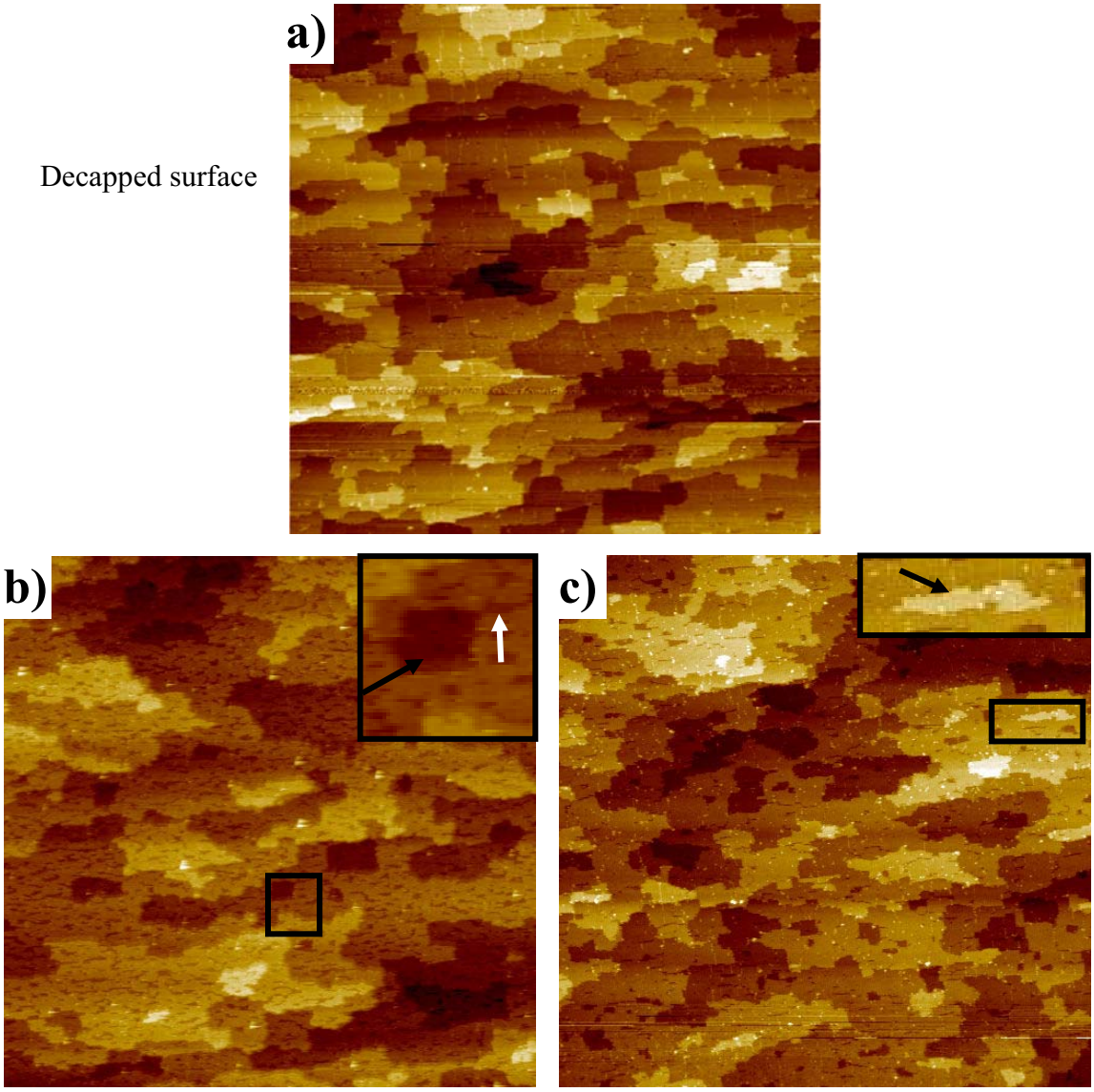



Figure 3: 500×500nm$^2$ filled state STM image of InGaAs a) decapped surface, b) 30 minutes air exposure followed by 30 minutes dose of atomic H at 380 ºC, and c) after high temperature anneal to 460-480 ºC. The terrace sizes improve with high temperature annealing. The atomic H dosed surface shown in (b) has a large density of dark surface features which are no longer present in (c). The inset in (b) includes large (black arrow) and small (white arrow) etch features caused by atomic H exposure. The inset in (c) includes a small terrace (black arrow) consistent with an incomplete terrace.

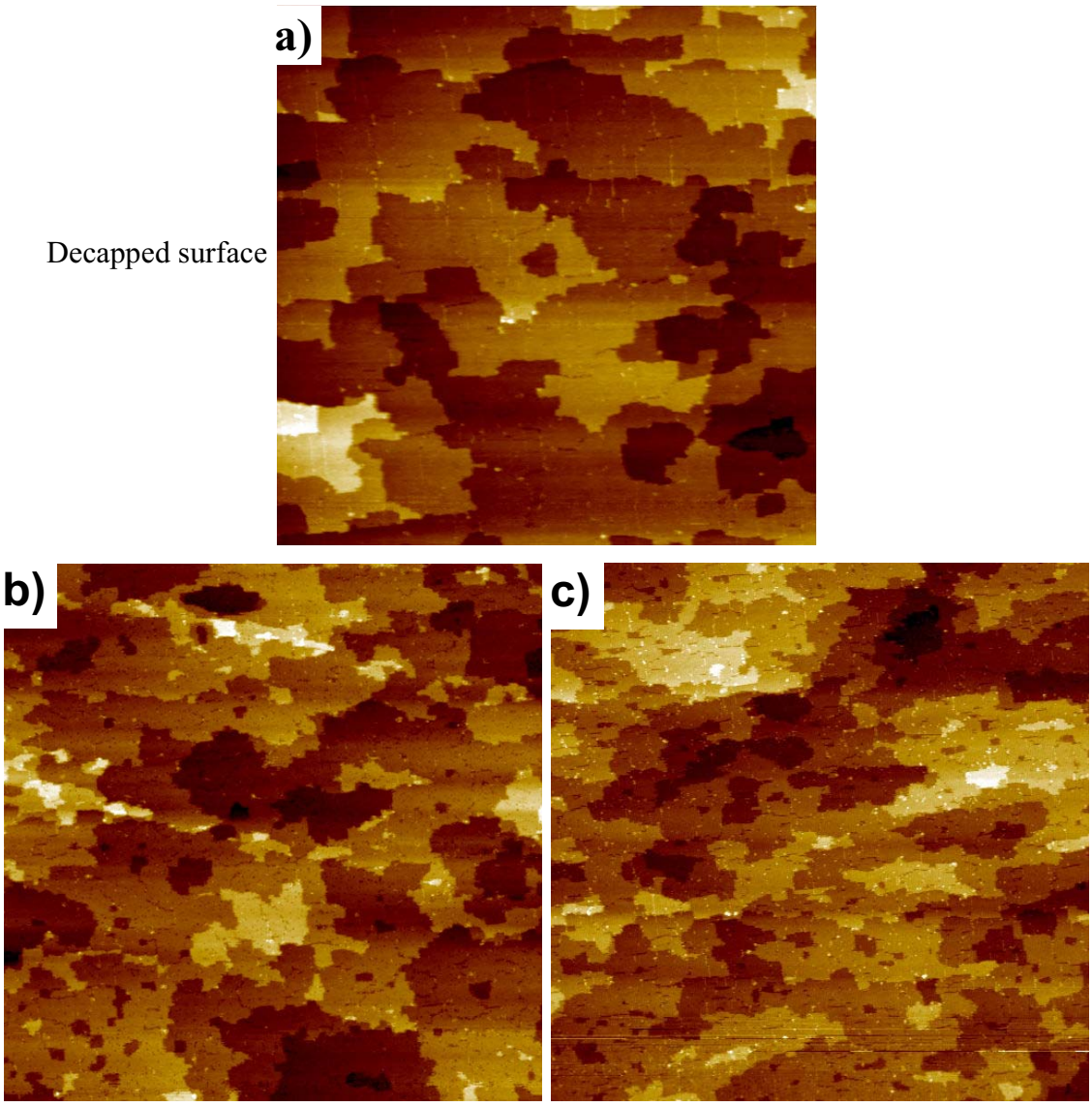
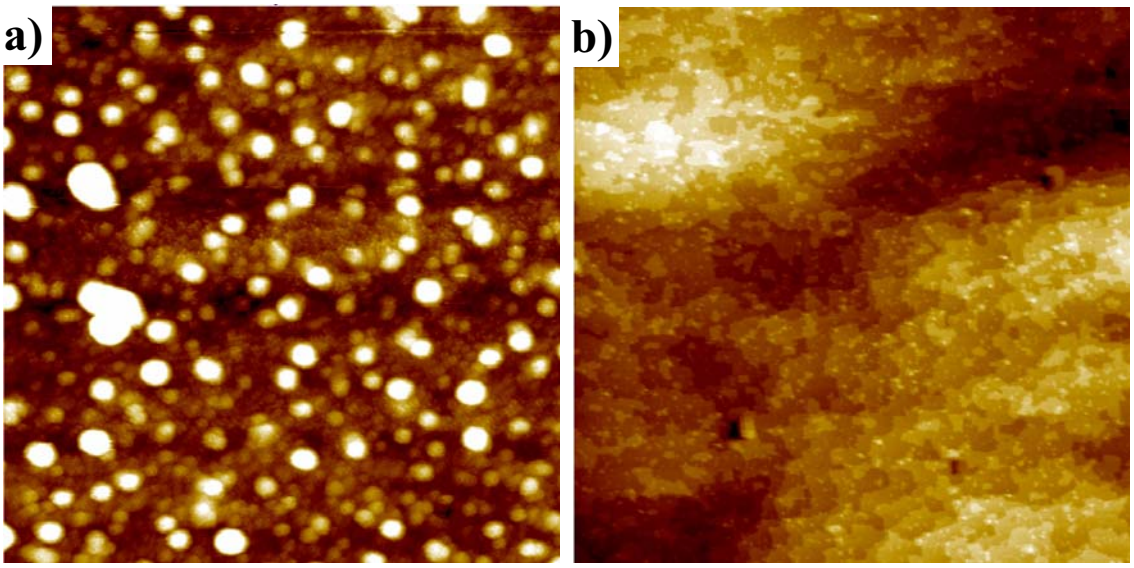



Figure 4: 500×500nm$^2$ filled state STM images of InGaAs a) a typical decapped InGaAs(001) surface, with a surface step coverage (SSC) of 5.66%. In the decapped surface, there are both dark etch like features and incomplete terraces. For STM images b)-c) all samples were decapping, exposed to air for 30 minutes, and atomic H cleaned at 380ºC and annealed at 460-480 ºC. b) A sample atomic H cleaned at 380 ºC for 5 minutes with SSC= 7.65%. Large increases in the dark etch features and incomplete terraces can be seen in comparison to the decapped surface. c) A sample atomic H cleaned at 380 ºC for 30 min with SSC=12.8%. The images are corrected for global tilt.

After atomic H exposure, the presence of etch features reduces the terrace sizes. There are two types of etch features, dark pits, inset Figure 3(b), which shows removal of surface atoms in the plane of the terrace and incomplete terraces, inset Figure 3(c), which illustrates a terrace that has been almost completely etched with only a residual amount remaining. Comparing the decapped sample to the 30 minute high temperature (HT)

dose without anneal sample, it is clear that there is a sharp increase in the etch pits. After a HT anneal, distinct improvement is observed in the surface morphology as shown in Figure 3(c). The atomic H cleaned and annealed surface has etch feature densities similar to that of the clean surface.

Besides etch pits, step edges are a major defect that can reduce carrier mobility in the channel, because steps usually contain dangling bonds due to the under-coordinated bonding configuration. Figure 4 compares air exposed samples cleaned with atomic H for 5 minutes vs. 30 minutes; both samples are annealed to 460 ºC after atomic H dosing. Using Scanning Probe Image Processor's (SPIP) grain analysis tool, the amount of the surface covered in edge features was quantified (step edges, horizontal and vertical defects). Typical decapped surfaces (Figure 4(a)) have a 5.6% surface coverage of step edges. A typical surfaces after a 30 minute air expose and 5 minute atomic H cleaning at 380 ºC followed by 460 ºC anneal have 7.6% surface coverage of step edges (Figure 4(b)), close to that of the decapped surface. Typical surfaces after a 30 minute air expose and a 30 minute atomic H cleaning at 380 ºC followed by 460 ºC have 12.8% surface coverage of step edges (Figure 4(c)), consistent with longer exposures generating more etch features.




30 min air exposure
30 min H dose @ -40 ºC
460-480 ºC anneal

30 min air exposure
200 ºC anneal
30 min H dose @ -40 ºC
460-480 ºC anneal

Figure 5: 500×500nm$^2$ filled state STM image of InGaAs a) dose with atomic H for 30 minutes at -40 ºC directly after exposure to air for 30 minutes. The images shows a high density of islands most likely unreduced oxide that was not full desorbed at low temperatures. b) STM image of a surface dose with atomic H at -40 ºC for 30 minutes with a 200 ºC anneal between air exposure and atomic H cleaning. The initial anneal before cleaning indicates the removal of water and other lower adsorbates can assist in the cleaning procedure.

Figure 5 shows STM images of atomic H cleaning at -40 ºC. Directly after exposure to air for 30 minutes, the sample was dosed with atomic H for 30 minutes

at -40 ºC with a final anneal of 460-480 ºC, Figure 5(a). The surface shows large bright islands probably from residual oxide left after the atomic H cleaning. At sub O°C temperatures, the surface will condense water which might not be able to desorb during atomic H cleaning at -40 ºC. However, if the sample is first annealed to drive off any residual water before cleaning, a -40 ºC atomic H cleaning results in a surface morphology similar to the RT atomic H cleaned surface. Figure 5(b) shows a surface exposed to air for 30 minutes then annealed to 200 ºC in UHV for 1.5 hours prior to atomic H cleaning for 30 minutes at -40 ºC with a final anneal of 460-480 ºC. The only major difference observed between the RT and the -40 ºC atomic H dose surfaces is the number of steps on a 500×500nm$^2$ STM image. The surface shown in Figure 5(b) is consistent with inhomogeneous etching during atomic H cleaning at -40 ºC.

The atomic H induced removal of the oxide layer involves multiple reactions. Atomic H can reduce $Ga_2O_3$ to $Ga_2O$ and $H_2O$ [20, 21, 32], and desorption of $Ga_2O$ occurs at ~400ºC [21, 37]. The influence of atomic H on In oxides has been assumed to be similar to that of Ga oxides [20]. Atomic H has been show to convert atomic As and $As_2O_3$ into $AsH_3$ and/or $H_2O$[38]. Atomic H at elevated temperature around 400 ºC is known to remove As on GaAs[20, 21]. Furthermore, the desorption of As oxides and $As_2/As_4$ occurs around 400 ºC [20, 21]. This atomic H induced volatilization of As is consistent with the reduction of any excess As defects on the atomic H clean surface. The absence of any oxides is likely due to the >300 Langmuir exposure which reduces any $Ga_2O_3$ or $In_2O_3$ to suboxides which are volatilized during annealing along with any As oxides.

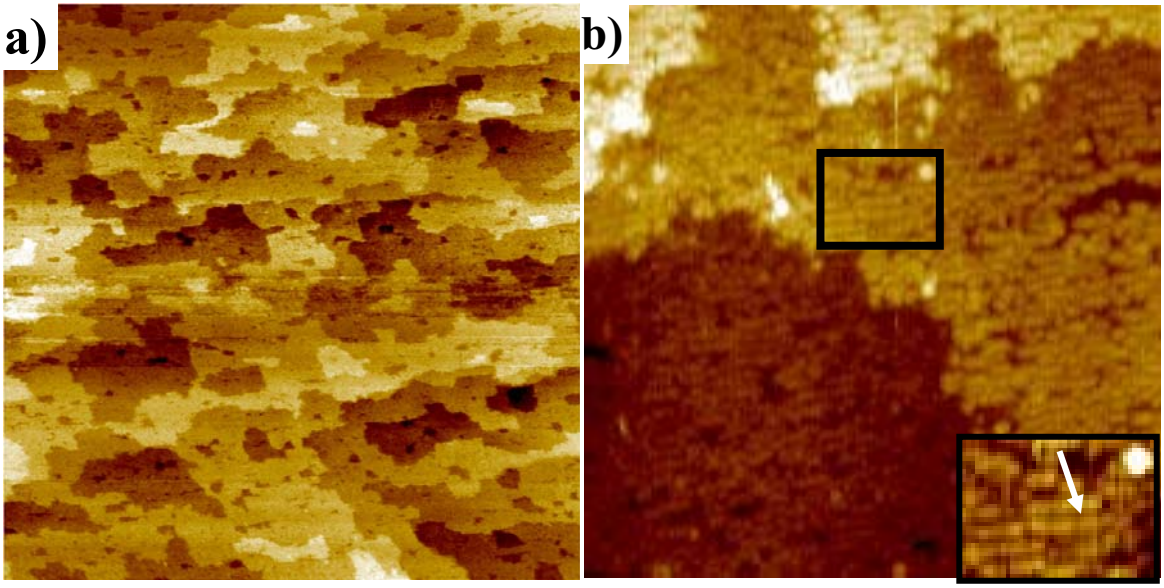
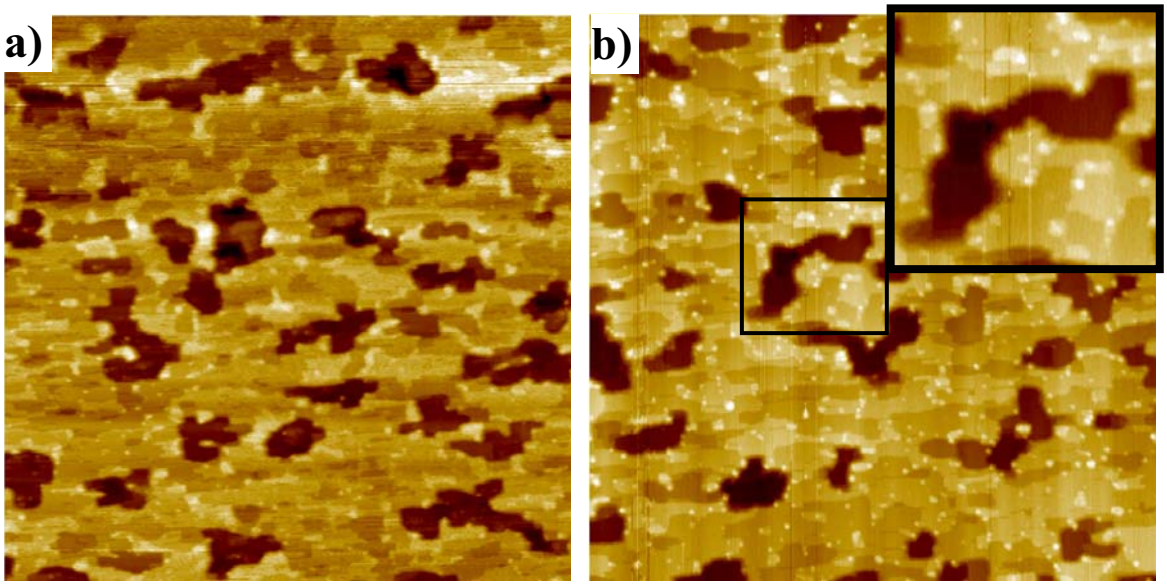



Figure 6: 40×40nm$^2$ filled state STM images of InGaAs surface after TMA dose at room temperature and annealed to 250 ºC. The inset shows an expanded view of 7×7nm$^2$ indicated by black square. The surface shows highly ordered horizontal row features (indicated by white arrow), consistent with a TMA induced surface reconstruction.

Following atomic H cleaning, the surface was exposed to TMA at room temperature and annealed to 250 ºC, an STM of the TMA dosed surface can be seen in Figure 6. Figure 6(a) shows a 500×500nm$^2$ STM image of the TMA dose on the atomic

H cleaned surface, showing a high nucleation density single monolayer film. The TMA induces a surface reconstruction creating a bulk like bonding configuration between the Al atoms and the surface As atoms[39]. A more detailing image is shown in Figure 6(b) The TMA passivation layer has horizontal rows of dimethyl aluminum. The surface is a highly ordered self-limiting layer that has high nucleation density. The self-limiting and high nucleation density are necessary for EOT scaling. The STM image of the TMA dosed surface is shown to satisfy key processing conditions: an atomically flat, high nucleation density, passivation layer; other scanning tunneling spectroscopy studies have shown this passivation layer unpins the Fermi level on InGaAs(001)-4×2 so the surface is electrically active [39].

InP: Figure 7(a) shows a STM image of InP after degassing an a 10 minute dose of atomic H at 380 ºC. The surface shows removal of the native oxide by atomic H exposure. The native oxide reduction by atomic H of InP, $InPO_4$, to $H_2O$, $PH_3$, $PH_2$, InH, and In has been reported in literature [40]. Others report the reductions of $InPO_4$, $In(PO_3)_3$, and $In_2O_3$ [26, 41]. Most reports are consistent with atomic H lowering the cleaning temperature for InP, and the exposure time for InP needed to clean the native oxide being longer than for GaAs. Five minute exposures to atomic H were also performed, not shown, which also had large bright features and partial coverage of the clean ordered surface. As shown in Fig 7, 10 minute exposures of InP to atomic H showed residual bright features that are most likely uncleaned oxide.




10 min H dose @ 380 ºC

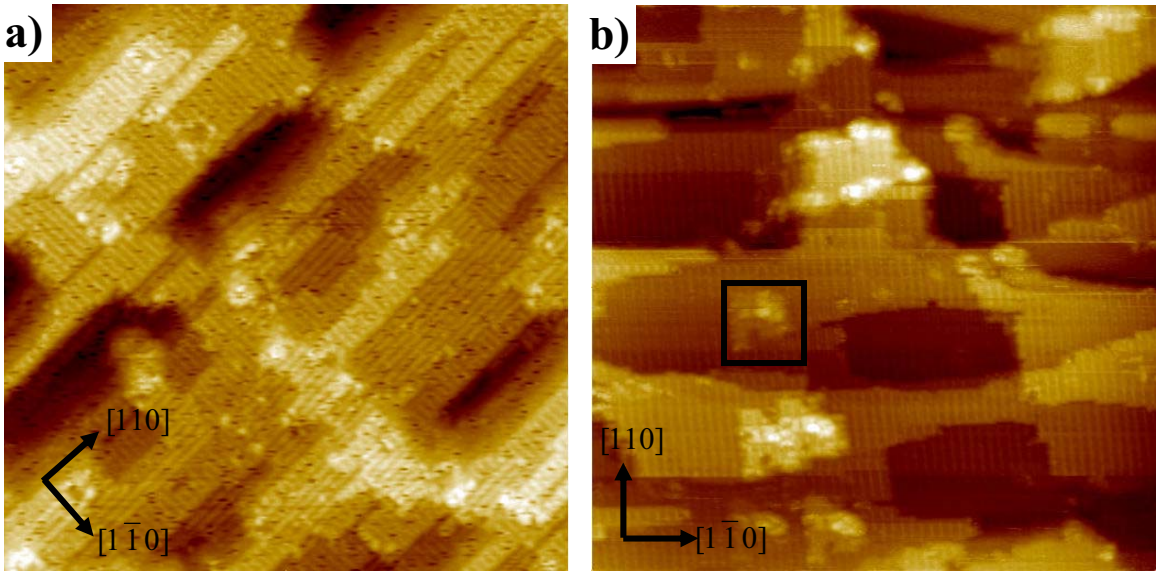
10 min H dose@380 ºC + 470 ºC anneal

Figure 7: 500×500nm$^2$ filled state STM image of InP a) after 10 minutes dose of atomic H at 380 ºC, and b) after 10 minutes dose of atomic H at 380 ºC plus a high temperature anneal to 470ºC. The STM images show an InP after atomic H exposure generates a flat surface with the large etch features. The density of the etch features does not significantly decrease with high temperature annealing. The inset shows an example of one etch features present on an InP sample.

After 10 minute atomic H dose and high temperature annealing the InP surface shows some etch features indicated by the inset in Figure 7(b). These etch features are different from that of InGaAs: they are much larger and deeper. Unlike InGaAs etch

features, these InP etch features do not decrease in density with a high temperature anneal to 470 ºC, Figure 7(b). The InP etch features could either be an etch pit to the InGaAs channel layer or impurities in the InP layer. The origin of these dark etch features is difficult to determine because a comparison to a decapped InP sample can not be performed. Fortunately, the density of the InP etch features can be controlled by the temperature during atomic H cleaning.

Other dosing parameters produced different surface reconstructions. Figure 8(a) shows a mixed surface reconstruction obtained after a 10 minute atomic H dose at 440 ºC. Conversely, after atomic H dosing at higher temperatures, 460-480 ºC, the results obtained show a single surface reconstruction, Figure 8(b). The surface reconstruction highly resembles that of the InGaAs(001)-(4×2) which is consistent STM of InP reported in literature [42]. Further studies on this surface are needed to ensure that at higher temperatures the InP layer is not fully etched and the remaining surface is the InGaAs channel.




10 min H dose @ 440 ºC

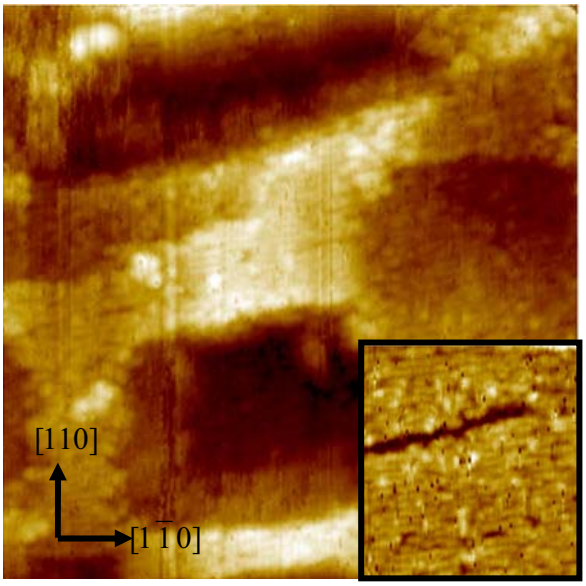
5 min H dose @ 460-480 ºC

Figure 8: 100×100nm$^2$ filled state STM image of InP a) 10 minutes dose of atomic H at 440 ºC, and b) 5 minute dose of atomic H at 460-480 ºC. The STM images shows, at lower dosing temperatures, a mixed surface reconstruction is obtained as shown by the mixture of rows along the [110] and [1 $\bar{1}$ 0] directions. Conversely, for higher temperature atomic H cleaning, a single surface reconstruction is observed with rows directed only along the [110] direction. The surface reconstruction highly resembles that of the InGaAs(001)-(4×2) which is consistent STM of InP reported in literature [42]. The black box in (b) indicates bright defect features. These bright defect features resemble incomplete terraces or material that did not properly arrange into the surface reconstruction.

Figure 9 shows STM images of an InP surface cleaned with atomic H for 5 minutes at 460-480 ºC and dosed with TMA at room temperature followed by a 250 ºC anneal. The InP surface after TMA exposure resembles that of the InGaAs surface after TMA exposure. The new ordered monolayer is perpendicular to that of the original InP

rows, and has 8Å spacing between the horizontal rows. An inset in Figure 9 shows the horizontal ordered monolayer more clearly.

The primary difference in surface quality between InP and InGaAs is the terrace sizes. With the present processing condition, the InP has slightly smaller terrace sizes. Furthermore, the atomic H cleaned InP(100) surface lacks the dark horizontal defects and the bright vertical defects observed on the decapped InGaAs surface. Conversely, the InP surface has more bright island features indicated by the rectangle in Figure 8.




TMA dose at RT
250C anneal

Figure 9: 40×40nm$^2$ filled state STM images of InP surface cleaned with atomic H for 5 minutes at 460-480 ºC after TMA dosing at room temperature and annealing to 250 ºC. The inset shows an expanded view of 25×25nm$^2$ image. The ordered surface reconstruction appears the same as the TMA dose on InGaAs.

## Conclusion

In summary, atomic H cleaning is able to restore InGaAs(001)-(4×2) surface after air exposure. With STM, the removal of the oxide layer and restoration of the clean InGaAs surface reconstruction is observed, allowing for a gate-last or replacement-gate process. The difference between room temperature and high temperature is minimal, allowing for a wide process window that must be optimized for etch rates compatible with the device structure. The key process, which is common to both room temperature and high temperature atomic H cleaning, is the high temperature anneal which reduces the step edge density and increases the terrace size. It is likely, the process can easily be implemented with other atomic H sources as long as the atomic H is free from high-energy ions and chemical contaminants.

Atomic H was also performed on a 2nm InP layer on top of the InGaAs channel. STM showed that variation of the temperature of the sample during atomic H cleaning had a strong effect on the surface reconstruction. After cleaning at high temperature, the

surface behaved very similar to that of InGaAs for TMA exposure, creating a highly ordered monolayer

## Acknowledgments

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