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Tip Cleaning and Sample Design for High Resolution MOSCAP x-KPFM

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Kelvin probe force microscopy (KPFM) is a unique technique that can provide two-dimensional potential profiles inside a working device. A procedure is described to obtain high-resolution KPFM results on ultra-high vacuum (UHV) cleaved III-V MOSCAPs. Two tip preparation methods: field emission and Cr coating show reproducible high spatial and energy resolution KPFM images. A unique sample design has been developed which is compatible with UHV cross-sectional KPFM (x-KPFM). Key design features are high density of devices on the cleave face, a buried device interface, and a cleavable gate contact. Using x-KPFM, the first UHV cleaved MOSCAP surface potential mapping is demonstrated.

Introduction

In order to effectively scale semiconductor devices, new techniques for device characterization are needed to image design operation on the nanoscale for both optimizations of device design and manufacturing. Kelvin probe force microscopy (KPFM) measures the two-dimensional potential profile of a surface [1]. KPFM can be used to probe passive and active devices, doping profiles [2], heterostructures [3,4], diodes [5,6], solar cells [7-9], etc. Cross-sectional KPFM (x-KPFM) in air of operational MESFETs [10,11] has been preformed. However, x-KPFM in ultra high vacuum (UHV) likely provides a more accurate image of the true potential inside working devices because it avoids surface oxidization and chemisorption that may influence the surface potential. The key requirements for x-KPFM as a practical method for probing nanoscale devices are (1) high spatial resolution, (2) high energy resolution, (3) samples compatible with external biasing and (4) samples designed to give flat cleaves in UHV. In the present paper, two tip preparation methods to achieve high spatial and energy resolution are reported. Energy resolution of better than 15 meV and spatial resolution better than 5 nm is demonstrated at a step edge of the InAs(110) surface with a potential peak induced by dangling bonds similar to that of GaAs(110) and GaP(110) [12]. In addition, an example

design for MOSCAP samples compatible with UHV x-KPFM, external biasing and flat cleaving is demonstrated.

Experimental Procedure

All experiments are performed in an Omicron VT-AFM/STM chamber with a base pressure 1-3 x 10^{-11} Torr and an attached preparation chamber with a base pressure 1-3 x 10^{-10} Torr. For KPFM, a conductive atomic force microscopy (AFM) cantilever is used. A bias is applied to the tip to minimize the electrostatic force between the surface and the tip caused by the contact potential difference (CPD). Conductive cantilevers are commercially available; however, these cantilevers are not atomically sharp (nominally tip radius ~15nm) because several layer of metal are usually coated over the silicon based cantilever. One of the simplest but less consistent ways of forming sharp tips is by gently crashing a silicon cantilever with a native insulating oxide into a sample surface to remove the native oxide while maintaining tip sharpness [13,14]. With field emission cleaning, it is possible to resharpen the apex after it has become dulled unless the cantilever has been damaged. Physical vapor deposition (PVD) is employed to deposit a few nanometers of metal onto sharp silicon cantilever to fabricate high-resolution KPFM cantilevers [15,16], but this method requires calibration experiments and high quality coating equipment. Both the tip cracking and the nanoscale metal coating methods are employed in the current study.

The first tip preparation method is tip cracking of the native oxide on silicon tips via field emission. Tip cracking is performed on the same commercially available highly doped silicon cantilevers from NANOSENSORs. In order to perform tip cracking in UHV, the tip holder is modified so that the silicon cantilever is grounded while in the tip carrier. The cantilever is first degassed for several hours at 150 °C in UHV. Afterwards, a tungsten filament is positioned close to the apex of the cantilever and with a high voltage (2 - 4 kV) is applied until a pressure burst and 5-20 μA of emission current are measured. The emission current is maintained for several seconds to allow for ample cleaning. After field emission the cantilever has adequate conduction and sharpness needed for high resolution KPFM.

The second, tip preparation method is coating of a silicon cantilever with an e-beam evaporator Cr. A SSS-NCHR cantilever from NANOSENSORs (having nominal tip radius less than 2nm) is coated with 3 to 5 nm of Cr. The coating extends from the apex to the contact for the applied bias. After coating, the tip is transferred to the UHV chamber and degassed for several hours at 150 °C in UHV. With the Cr coated cantilevers, topography and potential changes at the step edges on InAs(110) can be imaged simultaneously as seen in Fig. 1. Fig. 1c shows the topographic line profile of the step edge having height difference of 2Å which is very close to theoretical value, and the surface potential line profile shows a ~150 mV CPD increase at the step edge. The CPD increase at the step edge can be attributed to dangling bonds at the step edge; the CPD increase at step edges has also been observed in GaAs(110) and GaP(110) surfaces[12]. These results show that high spatial resolution, less than 5 nm, and high energy resolution, about 15 mV, have been achieved. Tips cleaned with field emission show similar resolution to the tips coated with Cr. Both of these tip preparation methods provide

adequate spatial and energy resolution required for performing x-KPFM on scaled MOSCAPs.

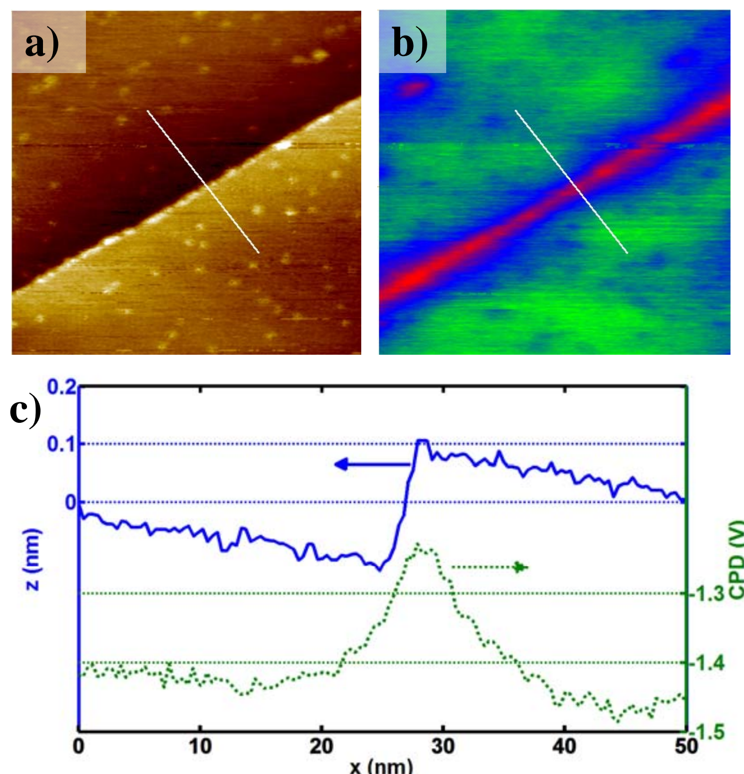

Figure 1: (a) 100 nm x 100 nm and (b) CPD of UHV cleaved InAs(110). (c) Line profiles indicated by the white line in (a) and (b) showing the topography and the potential spike at the step edge.

While the first requirement for high resolution KPFM is a sharp tip, the second requirement is a flat surface. In KPFM, the topology and CPD signals are independently measured insuring that under ideal conditions there is no influence on the measured CPD from the topology. However, scanning parameters (loop gain, frequency set point, and scanning speeds) need to be adjusted to compensate for the large topographical features thereby reducing the sensitivity of the CPD signal. Furthermore, large topographical features frequently damage the apex of the tip reducing the spatial resolution. In order to perform x-KPFM on an operational nanoscale MOSCAPs, a MOSCAPs design is needed which is both compatible with external biasing in UHV KPFM and which can be cleaved to provide flat surfaces.

The MOSCAP gate stack design used is illustrated in Fig. 2a. The gate stack is SiO_2/100 nm n^{++} GaAs/32 nm GGO/*n*-type GaAs. The 100nm n^{++} GaAs layer acts as the gate material for the MOSCAP structure. Degenerately doped n^{++} GaAs is chosen for the gate because it cleaves flat, allowing the gate to be included in the CPD image, and it provides ample conduction to minimize contact resistances. The SiO_2, GaAs, and GGO layers are blanket deposited. The SiO_2 is patterned allowing for a large 2 mm x 2 mm contact pads to be made through the to the n^{++} GaAs gate electrodes, Fig. 2b. A back side

contact is made to the semiconductor substrate. The SiO_2 layer is critical for two reasons: (a) the sample edge tends to have a rough cleave and (b) KPFM scanning at the edge of the sample is extremely abusive to the cantilever thereby reducing the resolution. The SiO_2 layer acts as a spacer between the edge of the sample and edge of the device, thereby, avoiding both edge roughness at the device and KPFM scanning at the edge of the sample.

For *in situ* cleaving for x-KPFM of MOSCAPs, the mechanical stability of the contacts and precisely controlling the location of the cleave face are critical. The sample is clamped into the sample holder making a stable contact to the backside contact and the frontside gate contact pad, Fig. 2c. Prior to introducing the sample to UHV, a nick is scribed on the top face of the sample to control the location of the cleave face. The sample is placed in UHV and degassed at 150 °C for several hours, and then cleaved at a temperature between -100 °C and 20 °C.

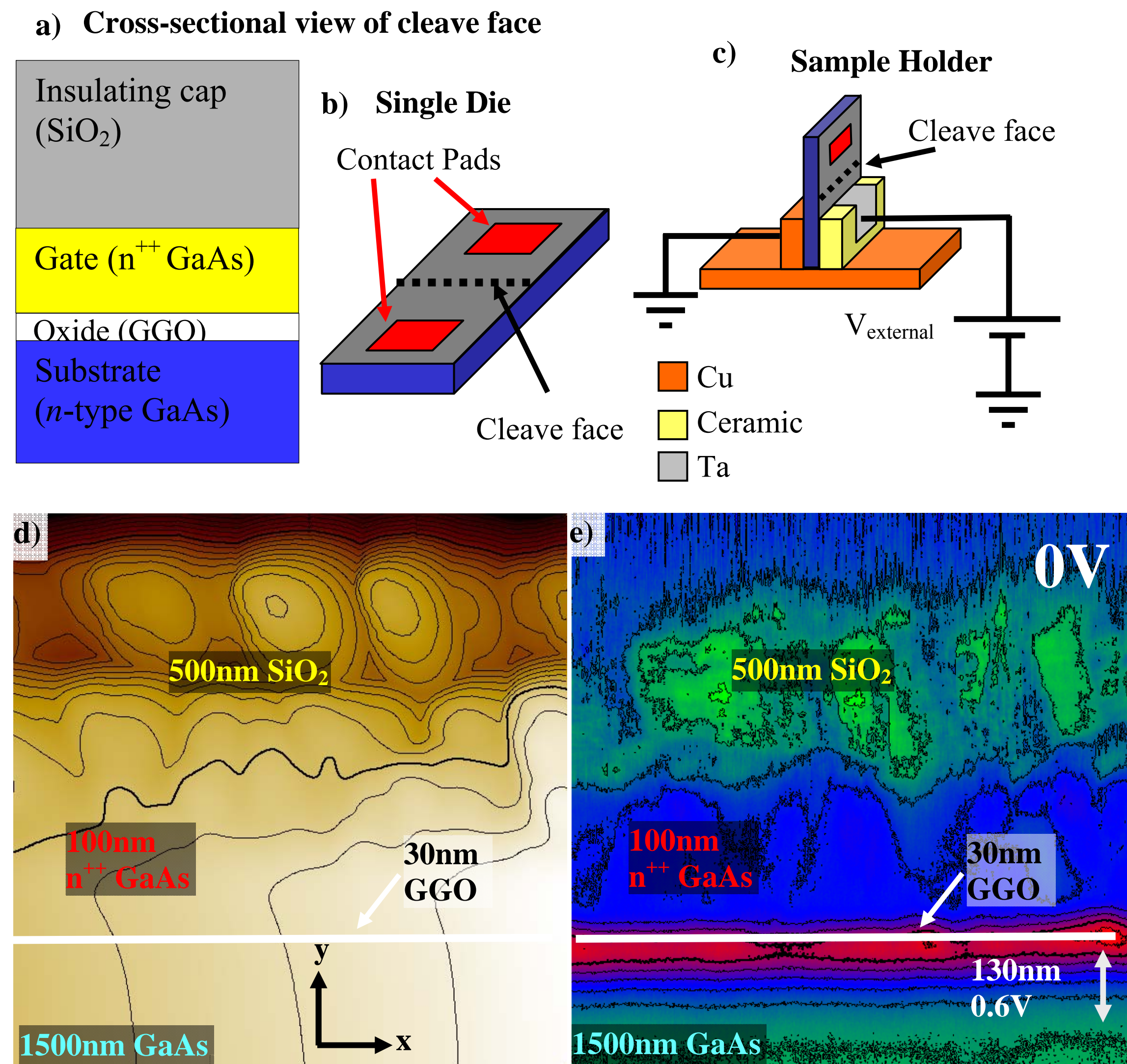

Figure 2: (a) Cross-sectional view of MOSCAP gate stack. (b) Top down view of a single sample die. Dashed line indicates location of nick on surface prior to entering UHV. (c) Schematic of the sample holder and external contacts. (d) 1000 nm ×1000 nm

topology image of UHV cleaved GaAs MOSCAP corresponding to the 0 V gate bias CPD image. Contour lines occur at 10 nm increments. (e) 1000×1000nm high resolution CPD image at 0 V gate bias. Contour lines occur at 100 mV increments.

Results and Discussion

A topology image from KPFM on the n^{++} GaAs/GGO/GaAs MOSCAP sample is shown in Fig. 2d (corresponding to the CPD image for 0 V gate bias Fig. 2e) at the MOS interface. A Cr coated SSS-NCHR cantilever is used for the cross-sectional KPFM. The contour lines in Fig. 2d occur at increments of 10 nm. The topology image shows that the n^{++} GaAs gate cleaves flat, allowing for the gate layer to be imaged with high resolution. Most of the topographical features are located in the SiO_2 layer showing that the insulating cap layer properly protects the MOS interface from cleaving damage. In the area of the MOS interface less than 10nm of topographical change occurs in the y-direction. The 30nm change along the x-direction is caused by the sample being slightly tilted in the sample holder, but this tilt does not significantly influence the scanning parameters required to achieve high resolution.

The very high-resolution two-dimensional CPD image in Fig. 2e of the 0V gate bias CPD map shows a depletion distance of 130nm, which is consistent with a lightly doped substrate. The high-resolution image also shows that the charge in the oxide is uniformly distributed. The potential changes in the semiconductor are expected to be confined to the depletion region directly under the oxide, so very little potential change should occur in the bulk substrate. The measured CPD shows a slight but negligible potential change in the substrate most likely caused by substrate resistance.

Several checks were performed to confirm the high-resolution image in Fig. 2e is an accurate representation of the charge in the gate oxide and the depletion region. An external bias was applied to the gate with respect to the substrate shown in Fig. 3. Fig. 3a shows 1000nm line traces at -1, 0 and +1V gate bias of n^{++} GaAs gate MOSCAP. The CPD of the n^{++} GaAs gate follows the applied bias, indicating ohmic contact between the metal contact pads and the n^{++} GaAs gate. High-resolution x-KPFM line traces in Fig. 3a show that the potential changes in the semiconductor channel are consistent with the depletion widths and barrier heights changing over the range of gate biases. The CPD profiles in Fig. 3a clearly show the typical electrical defects in the oxide. At 0V gate bias, the oxide has a positive bias with respect to the gate due to fixed charge. Full two-dimensional potential profiles of the planar MOSCAP structures can be seen in Fig. 3b. The contour lines in Fig. 3b occur at increments of 100 mV. The $CPD = \phi_{sample} - \phi_{tip} + V_{external}$, where ϕ_{tip} is the work function of the tip, ϕ_{sample} is the work function of the sample, and $V_{external}$ is the potential change caused by the external bias. The two-dimensional potential profiles in Fig. 3b also show a high density of contour lines at the n^{++} GaAs/GGO/GaAs interface, signifying that the potential drop is occurring over the oxide and/or the semiconductor channel.

The CPD profile, Fig. 3a, of the MOS interface corresponds to the expected work function offsets of n^{++} GaAs and *n*-type GaAs(110) surface. The cleaved GaAs(110)

surface is known to be unpinned [17,18]. The work function of *n*-type GaAs should be larger than the work function of n^{++} GaAs, which means the substrate should have a lower CPD value. The CPD of n^{++} GaAs is 0.18V larger than the substrate.

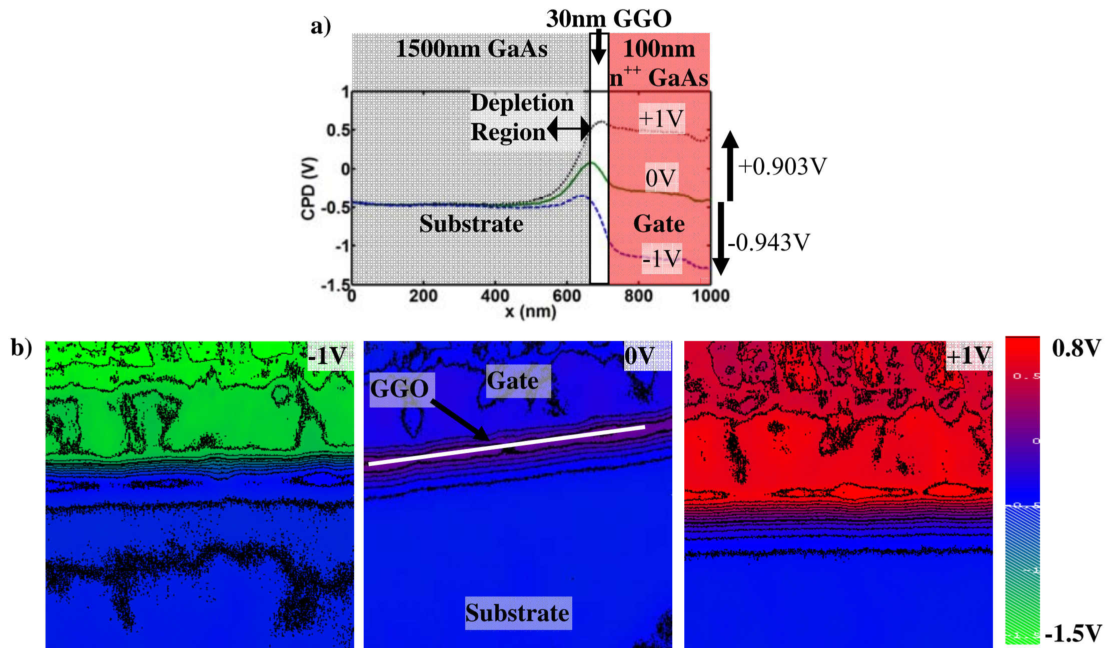

Figure 3: (a) 1000 nm line traces of n^{++} GaAs/GGO/ *n*-type GaAs MOSCAP at -1, 0, and +1V external gate bias. (b) 1000 nm ×1000 nm CPD images at -1V, (c) 0 V and (d) +1 V gate bias. Contour lines occur at 100 mV increments.

Conclusion

Two tip cleaning methods have been demonstrated showing high spatial and energy resolution for KPFM. High spatial resolution is critical for KPFM to be able to image potential profiles in scaled devices. A MOSCAP sample design for UHV x-KPFM was demonstrated. An insulating cap and a cleavable gate are incorporated into the MOSCAP design to improve the cleave face inside the MOSCAP thereby maintaining high KPFM resolution and low damage to the KPFM tip apex. The insulating cap embeds the devices thereby removing the active MOSCAP device from the edge of the sample. By using an n^{++} GaAs gate, the gate can also be included in the two-dimensional potential profile. The first operation UHV cleaved MOSCAP device imaged with KPFM is demonstrated, illustrating the potential changes from the external bias on the gate and semiconductor substrate. This work is a promising step toward further x-KPFM study of working MOSFETs device.

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